

Technological Progress in the Microprocessor Industry: Explanations of the Acceleration in 1990-2000 and the Slowdown in 2001-2008. *

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Abstract

The rate of technological progress in the microprocessor industry was higher during 1990-2000 when compared to 1971-1989. The acceleration in technological progress during 1990-2000 was followed by a slowdown during 2001-2008. I provide explanations for the acceleration and the slowdown by testing and verifying two hypotheses, (i) the acceleration was caused by an increase in the innovation rate in the upstream semiconductor equipment industry (ii) the slowdown was caused by a decrease in the technical efficiency of using the upstream innovations in microprocessor industry. The increase in the innovation rate in the semiconductor equipment industry during 1990-2008 was accompanied by an increase in R&D efficiency. A possible explanation for the increase in the innovation rate is that it was the outcome of efforts undertaken by SEMATECH, a government supported industrial research consortia established in 1988 to coordinate R&D in the semiconductor equipment industry.

1 Introduction

A number of studies seeking to explain the increase in productivity growth in the US economy during the second half of 1990s credit a central role to an acceleration in technological progress in the microprocessor industry during this period.¹ The cause of the acceleration has been debated in many academic, industrial and policy forums.² The rate of technological progress in the microprocessor industry slowed down after 2000. This paper provides explanations for the acceleration and slowdown by testing two hypotheses, (i) the acceleration was caused by an increase in the rate of innovation in the upstream semiconductor equipment industry (ii) the slow down was caused by a decrease in the technical efficiency of using these innovations in the microprocessor industry.

Jorgenson (2001) suggests an explanation closely related to hypothesis (i). He suggests that the acceleration was caused by a decrease in the product cycle in the semiconductor industry from 3 years to 2 years. An increase in innovation rate in the semiconductor industry results in a decrease in product cycle time, as shown in section 6.1 in this paper. The slowdown has been relatively less explored. Aizcorbe, Oliner, and Sichel (2006) suggest that the cause of the slowdown could not have been a reduction in product cycle time in the semiconductor industry. Flamm (2007) suggests hypothesis (ii), the slowdown occurred because the technology for using the innovations generated by the semiconductor equipment industry hit engineering problems that are insurmountable with the current state of technical knowledge in the microprocessor industry.

The studies above characterize the rate of technological progress in terms of the rate at which price per quality unit has declined for microprocessors.³ This approach however has the limitation, as noted in Aizcorbe, Oliner, and Sichel (2006) and Basu, Fernald, Fisher, and Kimball (2006), that changes in prices bought about by changes in demand and competitive conditions can be mistakenly inferred as changes in the rate of technological progress. To overcome this, I characterize the rate of technological progress in terms of the growth of a technological variable, microprocessor performance.⁴ Performance is a measure of how fast a microprocessor can execute software programs. Technological progress in the microprocessor industry is reflected as increases in performance. Nordhaus (2001) gives a detailed description of the use of performance as a measure of technological progress in computing, and compares it with the hedonic price based approach.

Figure 1 shows the performance of microprocessors produced by two main microprocessor companies, INTEL and AMD, during 1971-2008. The rate of technological progress, measured as the growth rate of performance, shows an increase in 1990-2000 followed by a decrease during 2001-2008. Figure 1 brings out that fact that the acceleration in the decline in price per quality unit, noted in Jorgenson (2001), Aizcorbe, Oliner, and Sichel (2006) and Flamm (2007) in 1990s

¹ Jorgenson (2001) was the first to point out the importance of microprocessor industry. See also Oliner and Sichel (2002) and Gordon (2001)

² See for example the proceedings of the workshop on Measuring and Sustaining the New Economy, organized by the Board on Science Technology and Economic Policy.

³ The price per quality unit is estimated using hedonic regressions.

⁴ Performance is the commonly used measure for comparing microprocessors in computer science . It is the reciprocal of the time that the microprocessor takes to execute a given set of programs.

Table 1: RATE OF TECHNOLOGICAL PROGRESS IN MICROPROCESSOR INDUSTRY

Company	Annual Performance Growth Rate(%)		
	1971-1989	1990-2000	2001-2008
INTEL	28.4	50.2	22.9
AMD	10.9	65.4	18.5

Source: Author

Industry	Annual Hedonic Price Index Decline Rate(%)		
	1988-1994	1994-2001	2001-2004
Industry	30.0	63.1	28.2

Source: Aizcorbe, Oliner, and Sichel (2006)

try.⁵ The focus in Aizcorbe and Kortum (2005) is on predicting the effect of changes in the arrival rate of new vintages on the evolution of prices. Hence they assume that new vintages arrive in a deterministic and continuous fashion, which leads the microprocessor firm to adopt new vintages continuously. In the model in this paper, new vintages arrive according to a Poisson process, hence adoption occurs at discrete random intervals, a feature that allows the data on adoption intervals to be used to infer changes in the arrival rate of new vintages.

The model in this paper is closely related to models that explore the effect of uncertainty on the timing of adoption of new technology, including Balcer and Lippman (1984), Dixit and Pindyck (1994), Doraszelski (2004), and especially Farzin, Huisman, and Kort (1998).⁶ The result in this paper that adoption of a new vintage occurs when the lag behind the frontier reaches a threshold value is common in all these models. While the focus in these papers is to theoretically understand how uncertainty associated with technological progress and market conditions affect the timing of new technology adoption, the focus in the current paper is empirical, to use the theoretical predictions of the technology adoption model to infer the causes of changes in adoption pattern and the rate of technological progress.⁷

This paper is closest in spirit to Griliches (1957), who uses a model of technology adoption

⁵ Section 2 elaborates on this link between technological progress in the microprocessor industry and the adoption of new vintages of semiconductor equipment.

⁶ For a good survey of models of technology adoption, see Hoppe (2002).

⁷ A macroeconomic model that is similar to the one in this paper is Parente (1999).

to understand the causes of variation in hybrid corn adoption pattern across different states in the US during 1932-1956. In a similar vein, this paper uses a model of technology adoption to understand the causes of an acceleration and slowdown that occurred in the rate of technological progress in the microprocessor industry during 1971-2008. One important difference with Griliches (1957) is that this paper explicitly incorporates how the efficiency of usage of the new technology influences the adoption pattern and the resulting rate of technological progress.⁸ In that respect the model in this paper shares many features with the model of General Purpose Technologies in Bresnahan and Trajtenberg (1995). The focus in Bresnahan and Trajtenberg (1995) is on how the institutional arrangements between the innovating sector and the using sector affects the rate of technological progress and welfare. This paper abstracts from institutional considerations and focuses on how changes in the technical efficiency with which the using sector uses the innovations affects the steady state rate of technological progress.

The model developed in this paper implies that in steady state the mean rate of technological progress in the microprocessor industry is determined by two parameters, the rate of innovation in the upstream semiconductor equipment industry and the technical efficiency with which microprocessor firms use these upstream innovations. This paper tests the hypotheses that the acceleration in 1990-2000 was the shift to a new steady state caused by an increase in innovation rate in the semiconductor equipment industry and the slowdown in 2001-2008 was the shift to a new steady state caused by a drop in technical efficiency of using these innovations in the microprocessor industry.

I use the implications of the model to statistically test for the shifts to new steady states. The model implies that in steady state the time intervals between a microprocessor firm's adoption of new vintages of semiconductor equipment would follow a gamma distribution, the scale parameter of the gamma distribution being the reciprocal of the rate of innovation in the semiconductor equipment industry. The test for equality of scale parameter in gamma distributions suggested by Shiue and Bain (1983) accepts the hypothesis that there was a change in the innovation rate in the semiconductor equipment industry during 1990-2008 when compared to 1971-1989. To test hypothesis (ii), I use the implication of the model that the choice of performance that maximizes profit when using a given vintage of semiconductor equipment, depends on the technical efficiency with which the microprocessor firms can use innovations embodied in new vintages. This allows technical efficiency of a microprocessor firm to be estimated from the data on performance and vintage of semiconductor equipment used. A Chow (1963) test for change in the estimated technical efficiency, accepts hypothesis (ii) that there was a decrease in technical efficiency of using the innovations during 2001-2008.

A unique contribution of this paper is that it uses the implications of the technology adoption model together with empirical estimates of the parameters to quantitatively decompose the changes in the rate of technological progress into contributions from changes in the innovation rate in the upstream industry generating the innovations and changes in technical efficiency in the downstream industry in using these innovations. The decomposition reveals that almost all of the increase in the rate of technological progress for INTEL microprocessors was caused by

⁸ Griliches (1957) mentions the importance adaptability of innovations in hybrid corn made in Corn Belt states to other states as a determinant of the adoption pattern. He refers to it as "Corn Beltiness" of different states.

the increase in innovation rate in the semiconductor equipment industry. For AMD, there was an improvement in technical efficiency also, which explains why the acceleration was more pronounced for AMD. The slowdown was caused almost fully by the decrease in technical efficiency of using the upstream innovations, for both INTEL and AMD. The R&D expenditure data of firms in the semiconductor equipment industry reveal that the increase in innovation rate in 1990-2008 was accompanied by an increase in R&D efficiency in the industry. Hence, a possible explanation is that the increase in innovation rate was the outcome of efforts undertaken by SEMATECH, a government supported industrial research consortia which was established in 1988, and has since spearheaded efforts to coordinate R&D activity and accelerate innovation in the semiconductor equipment industry.

This paper makes four contributions. First, in contrast to most models of technological progress, this paper quantitatively characterizes technological progress in purely technological terms, devoid of influence of prices. This provides a much cleaner foundation for isolating the causes of shifts in the rate of technological progress, by removing the confounding effect of changes in prices bought about by changes in demand and competitive conditions. Second, this paper provides an example of a method for detecting changes in innovation rate in an upstream industry based on changes in observable adoption patterns in the downstream industry. Third, this paper develops a model of the microprocessor industry, where technological progress is driven by adoption of new vintages of capital equipment. The model can be modified to apply to other products where adoption of new capital equipment drives technological progress. Fourth, this paper weaves together a coherent explanation for the acceleration and subsequent slowdown in technological progress in the microprocessor industry, from among the various suggestions that have been put forward in the literature.

I now turn to a brief description of the connection between technological progress in the microprocessor industry and innovations in the semiconductor equipment industry.

2 Technological Progress in the Microprocessor Industry - The link to the Semiconductor Equipment Industry

A microprocessor can be thought of as a combination of a basic electronic component, a transistor, and a method of organizing these transistors to perform operations like word processing or animation.⁹ The performance of a microprocessor can be increased either by increasing the speed of operation of the individual transistor or by organizing them in a more efficient way.¹⁰ The speed of operation of each individual transistor is limited by its size, smaller transistors are faster. The minimum size of each transistor is in turn limited by the quality of the semiconductor capital equipment used in manufacturing the microprocessor. Innovations in the semiconductor equipment industry lead to capital equipment that can make smaller transistors. Microprocessor firms like INTEL and AMD purchase this higher quality equipment and use them to produce higher

⁹ The method of organizing the transistors is called the *design* or *microarchitecture* of the microprocessor.

¹⁰ For a very good technical description of how smaller transistors and better microarchitecture determine the performance of the microprocessor, see Ronen, Mendelson, Lai, Lu, Pollack, and Shen (2000)

performance microprocessors. The ability of the higher quality semiconductor equipment to make smaller transistors confers another important benefit to microprocessor firms. If the size of the individual transistor is small, then more of them can be put on a given area, allowing microprocessor firms to implement new designs that increase performance. Innovations in the semiconductor equipment industry thus confers twin benefits to the microprocessor industry.¹¹

The evolution of microprocessor industry towards faster microprocessor traces the repeated adoption of higher quality vintages of semiconductor capital equipment. Each vintage of semiconductor capital equipment is marked by the size of the smallest transistor feature that it allows the microprocessor industry to make.¹² Thus the notion of vintage of capital has a precise physical interpretation here, that of length. Since these lengths are really small, they are usually quoted in microns (μ), which is a millionth of a meter. The leading microprocessor firm, INTEL, has adopted fourteen such vintages during 1971-2008, 10μ , 6μ , 3μ , 1.5μ , 1μ , 0.8μ , 0.6μ , 0.35μ , 0.25μ , 0.18μ , 0.13μ , 0.09μ , 0.065μ and 0.045μ . Figure 2, plots the different vintages of semiconductor capital equipment that INTEL and AMD have adopted against the date of adoption. The dates marked on the x-axis are the dates of adoption for INTEL.¹³

In the progression through these fourteen vintages from 1971-2008, the minimum feature size has decreased by a factor of 222.¹⁴ In Figure 2, it stands out that the time interval between the adoption of new vintages has become shorter on average since 1990. This is the reduction in technology cycle that has been noted in Jorgenson (2001), Aizcorbe, Oliner, and Sichel (2006) and Flamm (2007), and it forms the basis for hypothesis (i) in this paper.

In what follows I will use the letter ℓ to refer to each vintage of semiconductor equipment as well as its physical interpretation, the minimum feature size. The physical interpretation allows me to use ℓ as a measure of the quality of the semiconductor capital equipment, a lower ℓ implying a higher quality.

3 The Model

The model is in continuous time. I develop the model in a few stages starting with a description of the semiconductor equipment industry.

3.1 The Semiconductor Equipment Industry

The semiconductor equipment industry consists of a large number of firms which manufacture different types of optical, electrical, mechanical, and chemical machinery that microprocessor

¹¹ For a more elaborate description of how additional transistors confers benefits to microprocessor firms, see Intel (2005).

¹² The minimum feature size is referred to as *linewidth* in the industry.

¹³ I use the date on which INTEL (or AMD) released the first chip manufactured with that vintage as the date of adoption of the vintage.

¹⁴ To express in more practical terms, the innovations in semiconductor capital equipment have allowed microprocessor industry to go from manufacturing transistors of the $\frac{1}{8}$ th the size of a human hair to around $\frac{1}{2000}$ th of it.

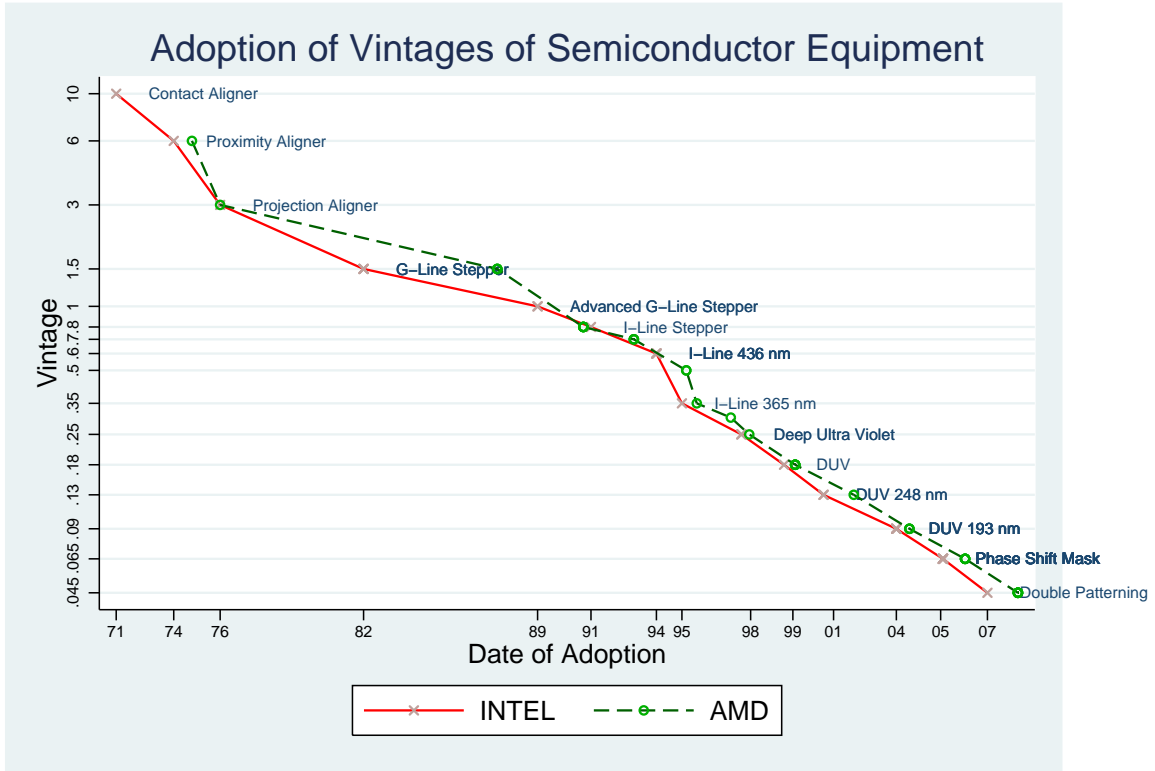


Figure 2: INTEL’s Adoption of new Vintages of Semiconductor Capital Equipment

manufacturers like INTEL and AMD require in their production.¹⁵ From the point of view of technological progress in the microprocessor industry, the most important function that these companies serve is that they undertake the R&D necessary to manufacture the next vintage of machines with a smaller ℓ . Hence I lump all these companies together as the semiconductor equipment industry, and assume that this industry undertakes the R&D necessary to reduce ℓ .¹⁶ This R&D generates innovations that follow a Poisson process with parameter λ . Each innovation reduces ℓ by a fixed factor δ , where $\delta < 1$. The highest quality vintage (i.e smallest ℓ) available at time t is denoted by the function $\bar{\ell}(t)$. I now turn to a description of the demand side of the model.

¹⁵ Some of the important firms in this industry are Applied Materials, Tokyo Electron, Nikon, Canon, ASML, Terdayne and Advantest. VLSI Research, a market research organization focussing on the semiconductor industry estimates the total revenue for the equipment industry in 2007 to be 57.5 billion dollars, 67% of which was accounted for by the top 15 companies. US companies accounted for 47% of the revenues of the top 15 companies, Japanese companies for 37% and European companies for 14%. See Semiconductor-International (2008)

¹⁶ The semiconductor equipment industry also has a separate classification under the North American Industrial Classification System (NAICS Code 333295) which makes it convenient to obtain the data on R&D expenditure done by the industry.

3.2 Demand in the Microprocessor Industry

Consumers care only about the performance of microprocessors. I assume a stationary inverse demand curve, given by,

$$\frac{p(t)}{m(t)} = D_0 [m(t)y(t)]^{\frac{-1}{\eta}} \quad (1)$$

Here $p(t)$ is the price of microprocessor sold at time t , $m(t)$ is the performance of the microprocessor and $y(t)$ is the number of microprocessors demanded. The price per quality unit is $\frac{p(t)}{m(t)}$ and $m(t)y(t)$ is the total number of quality units demanded. The basic assumption behind the demand structure is that total quality units demanded has a constant elasticity, η , in price per quality unit. One obvious abstraction in this demand specification is the absence of dynamic decision making by forward looking consumers. It is unlikely that a change in dynamic decision making process by consumers could have been a cause of the acceleration and slowdown, so I ignore this aspect of demand.¹⁷ I now describe the technology side of model.

3.3 Technology in the Microprocessor Industry

I use three equations to capture technology in this industry. The objective of this more elaborate than usual description of technology is to be able to formulate tests for the hypotheses (i) and (ii). Performance m depends on the vintage of semiconductor equipment ℓ , and on the number of transistors used T .

$$m(T, \ell) = m_0 \frac{T^\alpha}{\ell} \quad (2)$$

Here α is the technical efficiency of the microprocessor firm. It is a measure of the effectiveness of the microprocessor firm's method of organizing the transistors towards increasing microprocessor performance. Technical efficiency α , has a practical interpretation here, it is a measure of the quality of design developed by the microprocessor firm. Higher α means that the design is of a higher quality, it can be used to make a faster microprocessor with the same vintage of capital equipment (ℓ) and the same number of transistors (T). The test for hypothesis (ii), is implemented as a test for a shift in the value of α during 2001-2008. The fact that m is proportional to $\frac{1}{\ell}$ arises from the fact that smaller transistors are faster. Reducing ℓ by a given factor increases the speed of each transistor by the same factor. For a technical description of the relation between ℓ and m , see Ronen, Mendelson, Lai, Lu, Pollack, and Shen (2000) or Borkar (1999).¹⁸

¹⁷ See Gordon (2009) for a model of dynamic decision making and replacement cycles in the microprocessor industry.

¹⁸ "Every new process generation brings significant improvements in all relevant vectors. Ideally, process technology scales by a factor of 0.7 all physical dimensions of devices (transistors) and wires (interconnects) including those vertical to the surface and all voltages pertaining to the devices [4]. With such scaling, typical improvement figures are the following: 1.4 1.5 times faster transistors; two times smaller transistors...", Ronen, Mendelson, Lai, Lu, Pollack, and Shen (2000). The names "process generation" and "process technology" in the above quote are

I assume that unit cost of producing a microprocessor, c , has remained constant across different vintages. A central fact of this industry is that a fraction of microprocessors that are produced are defective because of manufacturing imperfections. A commonly used formula gives the fraction of good microprocessors in any given number as $e^{-\sigma S}$, where S is the physical size of the microprocessor and σ is a parameter that captures the degree of manufacturing imperfections.¹⁹ Hence the total variable cost of producing y good microprocessors is

$$VC(y, S) = cy e^{\sigma S} \quad (3)$$

The marginal cost of producing a microprocessor is $ce^{\sigma S}$ and is determined primarily by physical size S .²⁰ The third equation connects the equations (2) and (3), i.e. it fills in the missing link between performance of the microprocessor and the variable cost associated with its production. The link arises in a natural way in this setting, as the relationship between T and S . For a given vintage ℓ , the size of each transistor is proportional to $\frac{1}{\ell^2}$. Hence if the size of the microprocessor is S , the number of transistors that can be put on it using vintage ℓ machines is given by

$$T = T_0 \frac{S}{\ell^2} \quad (4)$$

Equation (4) links performance to cost and brings out the fundamental technology constraint facing a firm in making increasing the performance m of its microprocessors. As equation (2) shows, for a given vintage of semiconductor equipment ℓ , a firm can increase m only by increasing the number of transistors T that it is using in the microprocessor. But as shown in equation (4), for fixed ℓ increasing T increases S , because the microprocessor need to be of larger size to fit the additional transistors in. But increasing S increases the variable cost of producing the chip VC as shown in equation (3). Hence increasing m simply by increasing T leads to rapidly escalating variable cost of production, and is not a viable option for the firm. The only other way to increase m is to decrease ℓ , i.e. by adopting higher quality vintages of semiconductor capital equipment.

But adopting a new vintage of semiconductor capital equipment is not costless either. The rapidly increasing fixed cost of adopting a new vintage has been well documented in a number of sources.²¹ To capture this, I assume that moving to a smaller ℓ involves a fixed cost, $C(\ell)$, which

terms used in the semiconductor industry to refer to new vintage of semiconductor equipment. The reference mentioned in the above quote is Borkar (1999), who has a very good description of how reducing ℓ affects the different properties of the transistor including its speed. Borkar (1999) states that reducing ℓ by a given factor reduces *delay time* by the same factor, which is the same as increasing speed of transistor by the same factor.

¹⁹ The manufacturing imperfections arise because of contamination by dust particles. The larger the microprocessor the higher is the probability of it getting contaminated by dust, hence the fraction of defective microprocessors increases with size S . The parameter σ is called as the *defect density* in the semiconductor industry, and captures the susceptibility to contamination by dust particles. The formula for fraction good microprocessors (which is called *yield*) used in this paper, $e^{-\sigma S}$, is called the Poisson yield equation. See Berglund (1996) for a description of yield models in the semiconductor industry.

²⁰ “Cost is primarily determined by the physical size of the manufactured silicon die”, Ronen, Mendelson, Lai, Lu, Pollack, and Shen (2000). *Die* is the term used in the semiconductor industry to refer to a manufactured chip.

²¹ INTEL has estimated the cost of adoption next vintage of capital equipment (0.032μ) to be 7 billions dollars. See Intel (2009)

is increasing as ℓ becomes smaller. This fixed cost is intended to capture the cost of building a new fabrication plant, which often happens when there a new vintage is adopted, the cost of overcoming the manufacturing difficulties in getting a more complicated production process to work, and the cost of developing the new microprocessor design to be used with the new vintage.

Equations (2) and (4) can be combined as a single equation,

$$m = m_0 T_0^\alpha \frac{S^\alpha}{\ell^{1+2\alpha}} \quad (5)$$

This equation is the technology constraint facing a microprocessor firm. I now turn to a description of the profit maximizing problem facing a microprocessor firm.

3.4 Microprocessor Firm's Problem

I assume that the market for microprocessors consists only of a single firm facing the demand curve in equation (1). The data on AMD and INTEL microprocessors show that the optimal policies implied by this formulation are in agreement with the choices that both AMD and INTEL have made in the past.²² The explanations of the acceleration and slowdown provided in this paper are based on these optimal policies and hold equally well for AMD and INTEL. Moreover I provide evidence in section 7 that competition between AMD and INTEL is unlikely to have been the cause of the changes in growth rate of performance. In the light of these arguments, modeling the industry as a duopoly would only complicate the analysis without providing any additional help in finding explanations of the acceleration and slowdown.

I assume that the microprocessor firms sells only the highest quality microprocessor. As soon as a better product is made, the entire production is moved to this new product. This assumption helps focus on the factors that determine the rate at which microprocessor performance is growing. Given the Poisson arrival rate λ of innovations to semiconductor equipment that reduce ℓ by a factor δ , the microprocessor firm has to decide on the time path of performance of microprocessors and the number of microprocessors to be manufactured at each point in time. Increasing performance shifts the demand curve outward, increasing the variable profits (if marginal costs were not to change, which will be true as shown below).

The problem of the microprocessor firm is:

²² The technology constraints mentioned in section 3.3 are faced by both AMD and INTEL. In the plausible case that INTEL faces a demand curve of the type in equation (1) and AMD faces a residual demand curve of the same type, the profit maximizing problem faced by INTEL and AMD are identical, except for parameter values. This might explain why the optimal relationships implied by the model have been satisfied by the decisions that both INTEL and AMD have made in the past.

$$\begin{aligned}
& \max_{m(t), y(t), \ell(t), \{\tau_j\}_0^\infty} E \left[\int_0^\infty e^{-\rho t} [p(t)y(t) - cy(t)e^{\sigma S(t)}] dt - \sum_{j=0}^\infty e^{-\rho \tau_j} C(\ell(\tau_j)) \right] \\
& \text{subject to} \quad \frac{p(t)}{m(t)} = D_0 (m(t)y(t))^{\frac{-1}{\eta}} \\
& \quad \quad \quad m(t) = m_0 T_0^\alpha \frac{S(t)^\alpha}{\ell(t)^{1+2\alpha}} \\
& \quad \quad \quad \ell(t) \geq \bar{\ell}(t), \quad \bar{\ell}(0) \text{ given}
\end{aligned}$$

The term in the outer square brackets is the present discounted value of net profits, which is the difference between the present discounted values of gross profits (the integral in the objective function) and sum of fixed cost of adopting each vintage. The sequence $\{\tau_j\}_0^\infty$ are the times at which the firm decides to adopt the next vintage. The first constraint is the demand curve in equation (1), the next one is the technology constraint in equation (5) and the last simply states that the firm can at best be using the best vintage (smallest ℓ) currently available. I restrict $\eta > 1$ to make the firms's problem well defined.

The optimal choice of m and y depend only on the current value of ℓ . Hence I solve the problem by first solving the static problem of choosing m and y for a given ℓ and then embedding this solution back into the problem, to solve the dynamic problem of choosing the optimal times $\{\tau_j\}_{j=0}^\infty$ at which to adopt new ℓ . Substituting the constraints into the objective function, it can be seen that the solution to the static problem is as follows. Along an optimal path of m and y , the following condition has to hold.

$$\sigma S^*(\ell) = \alpha \quad (6)$$

The left hand side of the equation is the elasticity of variable cost with respect to S and the right hand side is the elasticity of revenue with respect to S . This optimality condition is the outcome of the tradeoff explained in section (3.3). Increasing S increases m and hence allows the firms to increase units sold y (or increase price p), thus increasing revenue. But increasing S also increases the variable cost because it results in a higher fraction of microprocessors being defective. The firm chooses S to balance these tradeoffs, resulting in equation (6) above. The equation implies that optimal size is $S^* = \frac{\alpha}{\sigma}$, independent of ℓ . Substituting the solution for S in equation (4) gives the optimal value of T as

$$T^*(\ell) = T_0 \frac{S^*}{\ell^2} \quad (7)$$

Hence T grows at twice the rate at which ℓ decreases. Substituting this in equation (2), gives the optimal performance as

$$m^*(\ell) = m_0 \frac{T^*(\ell)^\alpha}{\ell} = m_0 T_0^\alpha \frac{S^*}{\ell^{1+2\alpha}} \quad (8)$$

i.e. performance grows at $1 + 2\alpha$ times the rate at which ℓ decreases. The term $1 + 2\alpha$ shows the twin benefits from a smaller ℓ , mentioned in section 3. The exponent 2α represents the indirect

benefit of smaller ℓ on m through T , and the exponent 1 represents the direct benefit of smaller ℓ on m . The optimal number of microprocessors to produce $y^*(\ell)$ is,

$$y^*(\ell) = (\eta - 1) \frac{1}{ce^{-\sigma S^*}} \frac{\pi_0}{\ell^\varphi} \quad (9)$$

where π_0 and φ are given by

$$\begin{aligned} \pi_0 &= \left((\eta - 1) \frac{S^{*\alpha}}{ce^{\sigma S^*}} \right)^{\eta-1} \left(\frac{m_0 T_0^\alpha}{\eta} \right)^\eta \\ \varphi &= (1 + 2\alpha)(\eta - 1) \end{aligned}$$

Substituting the solutions for m and y into the demand equation (1) gives the optimal price as

$$p^*(\ell) = \frac{\eta}{\eta - 1} [ce^{\sigma S^*}] \equiv p^* \quad (10)$$

i.e. price of a microprocessor is a constant markup over the marginal cost of production, the term inside square brackets being the marginal cost of production. The solutions p^* and $y^*(\ell)$, gives the revenue along the optimal path as $r(\ell) = \eta \frac{\pi_0}{\ell^\varphi}$. As expected for a constant elasticity demand curve, the variable (gross) profits is a constant fraction $\frac{1}{\eta}$ of revenue, and is given by $\pi^*(\ell) = \frac{\pi_0}{\ell^\varphi}$. Using the optimal static policies in equations (6)-(10), the problem can be rewritten as

$$\begin{aligned} \max_{\ell(t), \{\tau_j\}_{j=0}^\infty} & E \left[\int_0^\infty e^{-\rho t} \frac{\pi_0}{\ell(t)^\varphi} dt - \sum_{j=0}^\infty e^{-\rho \tau_j} C(\ell(\tau_j)) \right] \\ \text{subject to} & \ell(t) \geq \bar{\ell}(t) \end{aligned}$$

I solve the problem using dynamic programming. The dynamic programming problem is most conveniently expressed by choosing the state variables as $\bar{\ell}$, the frontier technology, and $x = \frac{\bar{\ell}}{\ell}$, which captures how far the firm is behind the frontier. Note that $x < 1$, since the firm can adopt a vintage no smaller than $\bar{\ell}$. Since the innovation arrival is Poisson, the probability of one innovation arriving in a small interval of time Δt is $\lambda \Delta t$, and the probability of more than one innovation is approximately zero. Hence the value function should satisfy the Bellman equation

$$\begin{aligned} V(\bar{\ell}, x) &= \frac{\pi_0}{\left(\frac{\bar{\ell}}{x}\right)^\varphi} \Delta t + e^{-\rho \Delta t} [(1 - \lambda \Delta t) V(\bar{\ell}, x) \\ &+ \lambda \Delta t \text{Max} \{V(\delta \bar{\ell}, \delta x), V(\delta \bar{\ell}, 1) - C(\delta \bar{\ell})\}] \end{aligned}$$

The first term on the right hand side is the profit that the firm receives in a small interval of time Δt , the second term is the discounted expected payoff after Δt . With probability $1 - \lambda \Delta t$ no innovations arrive in which case the firm's value remains at $V(\bar{\ell}, x)$. With probability $\lambda \Delta t$ one

innovation arrives, in which case the firm has to choose between not adopting this innovation and getting value $V(\delta\bar{\ell}, \delta x)$ or adopting it and getting a value $V(\delta\bar{\ell}, 1) - C(\delta\bar{\ell})$.

Now I assume that $C(\ell)$ is homogeneous of degree $-\varphi$. While there is no direct empirical evidence for this, if this were not true then the factor by which ℓ shrinks would systematically vary over time, something which is not seen in the data (see section 5). This implies $V(\bar{\ell}, x)$ is homogenous of degree $-\varphi$ in $\bar{\ell}$, and hence $V(\bar{\ell}, x) = \bar{\ell}^{-\varphi}V(1, x) = \bar{\ell}^{-\varphi}v(x)$, where $V(1, x) = v(x)$. The dynamic program can thus be expressed with a single state variable, x . Re-writing with the single state variable, and taking the limit $\Delta t \rightarrow 0$, the Bellman equation simplifies to

$$\rho v(x) = x^\varphi \pi_0 + \lambda \left[\frac{1}{\delta^\varphi} \text{Max} \{v(\delta x), v(1) - C(1)\} - v(x) \right]$$

The left hand side of the equation is the payoff to owning the firm, which is the sum of the instantaneous payoff and the change in value which occurs if an innovation arrives, an event with hazard λ (taking account of the option to adopt). The optimal policy is to adopt a new vintage when the lag behind the frontier x , reaches a threshold values x^* (see Proposition 1 for proof). The threshold value x^* satisfies the following equation,

$$\rho(v(1) - C(1)) = \pi_0 x^{*\varphi} + \lambda \left(\frac{1}{\delta^\varphi} [v(1) - C(1)] - [v(1) - C(1)] \right) \quad (11)$$

Equation (11) is the value matching condition mentioned in Dixit and Pindyck (1994) and Farzin, Huisman, and Kort (1998). The firm adopts at the point where the value to adopting is equal to the value to waiting. The value to adopting immediately is the left hand side of the equation, the firms jumps to the frontier but it has to pay the fixed cost $C(1)$. The term on the right hand side is the value to waiting which is the sum of instantaneous payoff and the change in value that occurs if an innovation arrives at that moment in time. Equation (11) can be rewritten to give the threshold value x^* as

$$x^* = \left\{ \left(\rho + \lambda - \frac{\lambda}{\delta^\varphi} \right) \left(\frac{v(1) - C(1)}{\pi_0} \right) \right\}^{\frac{1}{\varphi}} \quad (12)$$

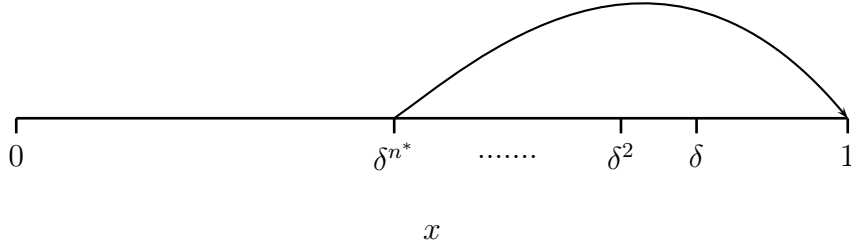
Equation (12) requires $\rho > \lambda \left(\frac{1}{\delta^\varphi} - 1 \right)$.²³ Since each innovation shrinks $\bar{\ell}$ by δ , this implies that it is optimal to adopt at every n^* th innovation, where n^* is the smallest integer such that $\delta^{n^*} \leq x^*$,

$$n^* = \left\lceil \frac{\ln(x^*)}{\ln(\delta)} \right\rceil$$

Hence scale factor is constant, δ^{n^*} . It is easy to summarize the dynamic policy using the simple diagram below. The possible values of x are $1, \delta, \delta^2, \dots, \delta^{n^*-1}$. Starting from $x = 1$, the value of x decreases to δ, δ^2, \dots , as the equipment sector produces its stream of innovations. When the n^* th innovation arrives, the firm adopts this and x becomes equal to one again, and this cycle repeats.

I summarize the results above. The microprocessor firm adopts every n^* th innovation made by the semiconductor equipment sector and hence ℓ used by the firm scales repeatedly by the same

²³ If discount factor ρ is not high enough, then discounted net profits are increasing over time and there will be no solution to the firm's problem.



factor δ^{n^*} . Even as ℓ decreases, the firm chooses to manufacture chips of size S^* independent of ℓ , increasing transistor count (T) and performance (m) in proportion to $\frac{1}{\ell^2}$ and $\frac{1}{\ell^{(1+2\alpha)}}$ respectively. The firm chooses to charge a constant price p^* per microprocessor, while increasing the number of units produced (y) in proportion to $\frac{1}{\ell^\varphi}$, where $\varphi = (1 + 2\alpha)(\eta - 1)$. Revenue and the variable (gross) profits also increase in proportion to $\frac{1}{\ell^\varphi}$.

This concludes the development of model. The next sections use the predictions from the model for the empirical application, to test hypotheses (i) and (ii) and investigate the causes of the acceleration and slowdown in technological progress. Before going into the tests, I briefly describe the dataset that has been created for this paper, and I verify the predictions of the model against data.

4 Data

The empirical part of this paper uses a new dataset of the microprocessor industry that has been created using data from a variety of sources. A detailed description of the dataset and the different sources is given in section (10). The dataset contains time series of characteristics of all INTEL and AMD desktop and laptop microprocessors, starting with the first microprocessor in 1971. There is a total of 588 microprocessors for INTEL and 457 for AMD.²⁴ The dataset contains the following characteristics for each microprocessor - product name, date of release, performance (m), vintage (ℓ), transistors (T), and size (S). The date of adoption of a vintage by a firm is taken to be the date of release of the first microprocessor using that vintage, by the firm. The next section compares the model's prediction to the data.

5 Empirical Verification of Predictions of the Model

The model also predicts that T and m , should increase as ℓ decreases, while S and the scaling factor $\frac{\bar{\ell}}{\ell}$ should not grow (or decline) with ℓ . In addition, the model predicts that T should grow twice as fast as ℓ . Figure 5 shows the evolution of T with ℓ for INTEL and AMD. As predicted,

²⁴ Among these, 135 microprocessors are in the low value category, which INTEL sells under the name Celeron and AMD under the name Sempron. These are usually defective parts which are sold at a low price. Hence I omit these microprocessors in this paper. This leaves a total of 453 microprocessors for INTEL and 351 for AMD. The server processors manufactured by INTEL and AMD have also been left out since functionally they are very different from desktop and laptop microprocessors.

T increases as ℓ decreases, and the slope is 2.34 for INTEL and 2.48 for AMD, close to the predicted value of 2. Figure 6 plots the evolution of m with ℓ . In line with the predictions of the model m increases as ℓ decreases. However, the slope of the curves can be seen to be changing over time, a point that becomes important in the explanation of the acceleration and slowdown in section 7.

Figure 7 show the evolution of S with ℓ for INTEL and AMD. The size S increases till around $\ell = 1.0\mu$ and then flattens out. The behavior of S after $\ell = 1.0\mu$ is consistent with the prediction of the model. The discrepancy before 1.0μ , which corresponds roughly to the period before 1985, arises from the fact that the defect density σ (see equation 3) increased during the period before 1985. As mentioned in section 3.3, σ is a measure of the degree of manufacturing imperfections present in the process of making the microprocessor. During the early years of the semiconductor industry in 1970s and 1980s, semiconductor companies learned to reduce the manufacturing imperfections by controlling the environment in the production facility, and as a result σ decreased during this period.²⁵ The size S that maximizes profits increases as σ decreases (see equation 6), and this explains the increase in S until early 1990s. Figure 8 plots the quantity σS against vintage ℓ . As can be seen from the figure, this quantity does not show any systematic variation with vintage ℓ . Although the parameter σ increased till late 1980s, I will ignore this variation in the model. An increase in σ would imply that m should have been growing at a faster rate during the period 1971-1989 than 1990-2000, and hence could not have been the cause of the acceleration. The cause of the acceleration more than compensated for the decrease in growth of σ after 1990. Figures 9 shows how the scaling factor $\frac{\bar{\ell}}{\ell}$ varies with ℓ for INTEL and AMD. The scaling factors also do not show any systematic variation with ℓ as predicted by the model.

The model makes one more testable prediction, that the microprocessor firm should adopt only occasionally, and should skip some innovations. In Figure(3), I plot the vintages adopted by INTEL and AMD (solid horizontal lines). The dotted lines are some of the vintages for which semiconductor equipment was sold by some of the leading semiconductor equipment producers (ASML, Nikon, GCA, SVGL, Parkin-Elmer and Ultratech), but were not used by INTEL. As can be seen from the graph, there were quite a number of vintages which neither INTEL or AMD adopted, in line with the prediction of the model.²⁶ Having verified that the predictions of the model are in agreement with the data, I turn to using the model to test the two hypotheses.

6 The Hypotheses Tests

I use the implications of the model to test the two hypotheses. From equation (8) it follows that the mean growth rate of m , which I denote by g_m , is $(1 + 2\alpha)g_\ell$, where g_ℓ is the mean growth rate

²⁵ For a good description of changes in σ in US semiconductor companies during 1970s and 1980s, see Cunningham (1990).

²⁶ The dotted lines are not the exhaustive list of all vintages. They correspond to only those vintages for which I could obtain data. The data for these were obtained from the websites of semiconductor equipment companies or from industry reports.

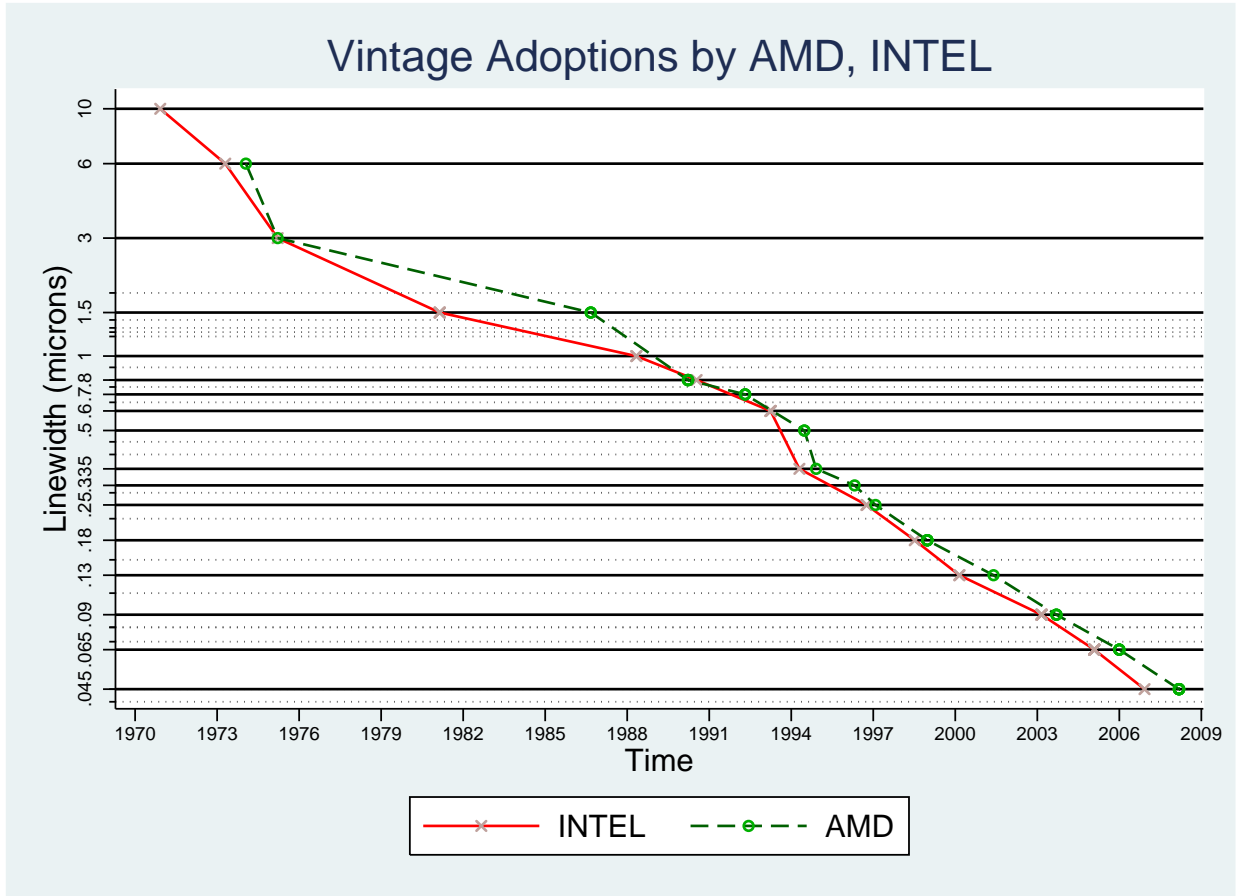


Figure 3: INTEL, AMD do not adopt all vintages.

of ℓ . Since ℓ follows a Poisson process with rate λ and stepsize δ , $g_\ell = -\lambda \ln(\delta)$, where I have put the negative sign because ℓ is decreasing over time ($\ln(\delta)$ is negative). This gives the mean growth rate of m as

$$g_m = (1 + 2\alpha)\lambda \ln(\delta) \quad (13)$$

The first term $1 + 2\alpha$ can be thought of as the contribution made by the microprocessor firm (INTEL or AMD) to the growth of microprocessor performance and the second term $\lambda \ln(\delta)$ can be thought of as the contribution made by the semiconductor equipment companies. The two hypotheses are in qualitative agreement with the predictions of the model, since an increase in λ causes an increase in g_m (hypothesis (i)) and a decrease in α , causes a decrease in g_m (hypothesis (ii)). I now describe the statistical tests for the two hypotheses.

6.1 Test of Hypothesis (i)

Let λ_1 be the innovation rate during 1971-1989 and λ_2 during 1990-2008. Then the null hypothesis and alternate hypotheses are $H_0 : \lambda_2 = \lambda_1$ and $H_1 : \lambda_2 \neq \lambda_1$ respectively. The test is based on the distribution of the time intervals between the adoption of consecutive vintages. Let $\Delta\tau_k$ be the k^{th} adoption interval, i.e. the time interval for which the firm operates with the k th vintage of semiconductor equipment. Then the optimal policy implies that $\Delta\tau_k$ is the time required for n^* events to happen, the events being generated according to a Poisson process with rate parameter λ . It follows that $\Delta\tau_k \sim \mathbf{G}(n^*, \frac{1}{\lambda})$, where \mathbf{G} is the gamma distribution with p.d.f given by

$$g(\tau) = \frac{\lambda^{n^*} (\tau)^{n^*-1} e^{-\lambda\tau}}{\Gamma(n^*)}$$

The first parameter of the gamma distribution (shape parameter) is equal to n^* , the adoption policy of the firm. The second parameter (scale parameter) is equal to $\frac{1}{\lambda}$. The idea is to test for the equality of the scale parameter in two samples, the first sample containing adoption intervals $\Delta\tau_k$ that occurred during 1971-1989 and the second sample containing those that occurred during 1990-2008. The procedure of the test however, would depend on how the adoption policy n^* has changed between the two periods, and specifically whether n^* would change in response to a change in λ .

As mentioned in section 5, the factor by which ℓ has scaled do not show any tendency in data to grow or decline with ℓ . The factor by which ℓ scales corresponds to δ^{n^*} in the model, hence data suggests the shape parameter n^* is equal across all periods. In consonance with the data, the model also predicts that n^* will change in response to λ only if the change in λ is sufficiently large, i.e there are intervals of λ over which n^* does not change (see Proposition 2 for proof).²⁷ Since the data suggests that there was no change in n^* and since the model implies that it is possible that n^* does not change in response to change in λ , I will assume that n^* has remained the same across the two periods. Hence the hypothesis can be verified using a test for the equality of the scale parameters in two samples under the assumption that the shape parameter has not changed.

I use the test suggested in Shiue and Bain (1983). Consider two samples of size N_1 and N_2 drawn from gamma distributions $\mathbf{G}(n^*, \frac{1}{\lambda_1})$ and $\mathbf{G}(n^*, \frac{1}{\lambda_2})$ respectively. Then, under H_0 ,

$$\frac{\Delta\bar{\tau}_1}{\Delta\bar{\tau}_2} \sim \mathbf{F}(2n^*N_1, 2n^*N_2) \quad (14)$$

where $\Delta\bar{\tau}_1$ and $\Delta\bar{\tau}_2$ are the means of the adoption intervals from the two samples (see Proposition 4 for proof). The test statistic, $\frac{\Delta\bar{\tau}_1}{\Delta\bar{\tau}_2}$ is easily calculated. Note that the rates λ_1 and λ_2 do not enter the parameters of the \mathbf{F} distribution.

²⁷ If λ increases and n^* does not change, then the expected time interval between adoptions, $\frac{n^*}{\lambda}$, would decrease, i.e on average the firm would adopt more frequently. This observation is in agreement with the reduction in technology cycle mentioned in Jorgenson (2001).

Table 2: RESULT OF TEST FOR HYPOTHESIS (i)

Sample 1	Sample 2	N_1	N_2	Distribution	F-Statistic	p-value
1971-1989	1990-2000	4	9	F(32,72)	2.085	0.0052
1990-2000	2001-2008	5	4	F(40,32)	1.024	0.477

The data for the test is shown in Table 14. I use the data from only INTEL for this test. AMD was a laggard in this industry in early years, especially in adoption of new vintages. The adoption lags for AMD are unusually large in the earlier years, especially when compared with INTEL's adoption or with industry reports of when the vintage became available. In total, INTEL made fourteen adoptions of semiconductor equipment. The adoption dates, and the adoption intervals calculated from these dates, are shown in the table. The value of n^* is needed to know the distribution of the test statistic. I use the maximum likelihood estimate of n^* , using the data pooled from both samples. In the problem for maximizing the likelihood that the adoption intervals come from a gamma distribution, the first order condition with respect to λ implies that the following condition has to hold at the maximum,

$$\hat{\lambda} = \frac{\hat{n}^*}{\Delta\bar{\tau}} \quad (15)$$

where $\Delta\bar{\tau}$ is the mean adoption interval in the pooled sample (see Proposition 5 for proof). The fact that n^* is an integer greatly simplifies the estimation. For integer values of $n^* = 1, 2, 3, \dots$, the value of $\hat{\lambda}$ is calculated using equation (15). With these values of n^* and $\hat{\lambda}$, the value of the likelihood is calculated. The (n^*, λ) pair, that gives the maximum value of likelihood is the MLE estimate. This procedure gives $n^* = 4$, implying that INTEL adopts every fourth innovation that the semiconductor equipment industry produces.

The result of the test is in the first row of Table 2. Hypothesis H_0 a p-value of 0.0052 and is rejected even at a 1% significance level. The second row shows the result of the test with observations in 1990-2000 and 2001-2008 as the two samples. The hypothesis that there is no change in λ between 1990-2000 and 2001-2008 has a p-value of 0.477 and cannot be rejected.

Estimating λ using equation (15) for the three periods separately, gives $\lambda_1 = 0.92$, $\lambda_2 = 1.90$ and $\lambda_3 = 1.92$. Thus innovation rate in the semiconductor industry more than doubled after 1990. The change in the innovation rate can be compared with the reduction in the technology cycle from 3 years to 2 years mentioned in Jorgenson (2001). The expected adoption interval (technology cycle) in this model is the mean of the gamma distribution $\mathbf{G}(n^*, \frac{1}{\lambda})$, which is equal to $\frac{n^*}{\lambda}$. Using the estimated value of $n^* = 4$, and $\lambda = 0.9$ for the period 1971-1989, the mean adoption interval is 4.4 years. Similarly, with $\lambda = 1.90$, the mean adoption interval for 1990-2008 is 2.1 years. In agreement with Jorgenson (2001), the adoption interval has shortened. The

adoption interval of 4.4 years during 1971-1989 is larger than the 3 years mentioned in Jorgenson (2001). One possible explanation for this is that the first adopters of semiconductor equipment during the years 1971-1989 was DRAM producers and not microprocessor producers, and the 3 year cycle mentioned in Jorgenson (2001) could reflect the adoption cycle followed by DRAM producers. In the later years, microprocessor firms adopted at the same time, if not earlier, than DRAM producers. Hence the estimate λ_1 is possibly slightly higher than 0.9. This explanation can be checked with the data on DRAM production, and points to a possible future area of research.

The analysis above confirms that there was an increase in the rate of innovation λ in the semiconductor equipment industry. But the analysis does not provide an explanation of what might have caused the increase in λ . I postpone an explanation to section 7, and move on to the test of hypothesis (ii).

6.2 Test for Hypothesis (ii)

Let α_1 be the technical efficiency of the microprocessor firm during 1971-2000 and α_2 during 2001-2008. Then the null and alternate hypotheses are $H_0 : \alpha_2 = \alpha_1$ and $H_1 : \alpha_2 \neq \alpha_1$ respectively. I use the relationship implied by the model between m , ℓ and α for the test. Equation (8) implies that α can be obtained from the regression

$$\ln m = a_0 + a_1 \ln \ell \quad (16)$$

as $\alpha = \frac{a_1 - 1}{2}$. The hypothesis is tested using the test suggested in Chow (1963) for detecting changes in estimates of linear regression. Applying Chow (1963) to the regression equation (16) implies that the test statistic

$$\frac{\frac{RSS_c - (RSS_1 + RSS_2)}{k}}{\frac{RSS_1 + RSS_2}{N_1 + N_2 - 2 * k}}$$

is distributed $\mathbf{F}(k, N_1 + N_2 - 2 * k)$ where RSS_c is the residual sum of squares from the regression using the data from both samples, RSS_1 and RSS_2 using only from sample 1 and sample 2 respectively, k is the number of regressors which is equal to 2 here, and N_1 and N_2 are the sizes of sample 1 and sample 2 respectively. Table 15 shows the data that is used for the test. For each vintage ℓ , there are a number of microprocessors produced, and hence there is a dispersion of m . I use the average performance of all microprocessors in a vintage for the test. The application of the Chow test requires the errors to be homoscedastic, and I confirm this with the Breusch-Pagan test. The square of residuals, ϵ^2 , from the regression in equation (16) (using data from both samples together) is regressed on a constant and $\ln \ell$. The coefficient on $\ln \ell$ is not significant, for both INTEL and AMD, and hence errors are homoscedastic and Chow test is applicable.²⁸

The p-values for the test are shown in Table 3, the first row for INTEL and second row for AMD. For INTEL H_0 has a p-value of 0.036 and is rejected at a 5% significance level. For

²⁸ The t-statistic on $\ln \ell$ for INTEL is -1.47 and for AMD is -0.98

Table 3: RESULT OF THE TEST FOR HYPOTHESIS (ii)

Company	Sample 1	Sample 2	N_1	N_2	Distribution	F-Statistic	p-value
INTEL	1990-2000	2001-2008	5	4	F(2, 5)	6.95	0.0359
AMD	1990-2000	2001-2008	7	4	F(2,7)	83.03	0.0001
INTEL	1971-1989	1990-2000	5	5	F(2, 6)	2.38	0.1739
AMD	1971-1989	1990-2000	3	7	F(2, 6)	43.62	0.0003

AMD the hypothesis is rejected even at a 0.1% level. The third and fourth rows show the result of the same test, but between periods 1971-1989 and 1990-2000. The hypothesis that there was no change in α between 1971-1989 and 1990-2000 cannot be rejected for INTEL at a 5% level, while it is strongly rejected for AMD. The values of α estimated for INTEL and AMD for the three periods are shown in Table 4. The estimates are significant for both AMD and INTEL for all three periods. As can be seen from Table 4, between 1990-2000 and 2001-2008, α dropped from 0.78 to 0.19 for INTEL and from 1.35 to 0.02 for AMD.

Table 4: ESTIMATES OF α

Period	INTEL			AMD		
	a_1	α	R^2	a_1	α	R^2
1971-1989	-2.10 (0.37)	0.55	0.92	-0.76 (0.5)	-0.12	0.71
1990-2000	-2.56 (0.22)	0.78	0.98	-3.70 (0.12)	1.35	0.99
2001-2008	-1.38 (0.06)	0.19	0.99	-1.048 (0.11)	0.02	0.94

Having verified that the technical efficiency, α , decreased for both AMD and INTEL during

Table 5: ESTIMATES OF λ and α

Variable	Company	1971-1989 (I)	1990-2000 (II)	2001-2008 (III)
$g_m(\%)$	INTEL	28.4	50.2	22.9
	AMD	10.9	65.4	18.5
λ	Equipment Industry	0.90	1.92	1.90
α	INTEL	0.66	0.77	0.17
	AMD	0.01	1.35	0.02

2001-2008, I provide an explanation for the decrease in next section.

7 Explanations for the Acceleration and Slowdown

The test for hypothesis (i) confirms that there was an increase in λ during 1990-2008, and the test for hypothesis (ii) confirms that there was a decrease in α , during 2001-2008. Equation (13) shows that the former could have caused the acceleration and the latter could have caused the slowdown. But to what extent were these the only causes? More importantly, what caused the increase in λ in 1990-2008 and the decrease in α in 2001-2008? I answer these two questions in this section.

The starting point of the analysis is the expression for g_m above. For two time periods t and t' ,

$$\frac{g_{m_t}}{g_{m_{t'}}} = \left(\frac{\lambda_t}{\lambda_{t'}} \right) \left(\frac{1 + 2\alpha_t}{1 + 2\alpha_{t'}} \right) \quad (17)$$

since δ is assumed to be the same across all periods. The change in growth rate across two periods is the product of two terms. The first term $\frac{\lambda_t}{\lambda_{t'}}$ is the contribution of semiconductor equipment companies, because of changes in the innovation rate in the semiconductor equipment industry. The second term $\frac{1 + 2\alpha_t}{1 + 2\alpha_{t'}}$ is the contribution of the microprocessor company, because of change in technical efficiency of using the innovations. The estimates of α and λ for the three periods, in conjunction with equation (17) can be used to quantitatively decompose the changes in g_m . I reproduce in Table 5 the growth rates g_m in the data, together with the estimates of λ and α for the three periods. In the following sections, the subscript I, II and III refers to time periods 1971-1989, 1990-2000 and 2001-2008 respectively.

Table 6: CONTRIBUTIONS TO ACCELERATION IN GROWTH OF MICROPROCESSOR PERFORMANCE

		INTEL	AMD
Acceleration (data)	$\frac{g_{mII}}{g_{mI}}$	1.79	6
Contribution of Equipment. Co.	$\frac{\lambda_{II}}{\lambda_I}$	2.08	2.08
Contribution of Microprocessor. Co.	$\frac{1 + 2\alpha_{II}}{1 + 2\alpha_I}$	1.09	3.62

7.1 Explanation for the Acceleration

Table 6 shows the decomposition of the increase in g_m , using the estimates in Table 5.

Comparing 1973-1989 to 1990-2000, g_m increased by a factor of 1.79 for INTEL. The contribution from semiconductor equipment industry increased by a factor of 2.08 and the contribution from INTEL increased by factor of 1.09. Hence, the contribution to the acceleration of performance growth for INTEL was overwhelmingly from the semiconductor equipment industry, and very little was accountable to improvements in INTEL’s technical efficiency. The two contributions taken together account for more than the 1.79 factor increase in performance seen in the data, and this discrepancy must be taken to be the result of factors not taken into consideration in this model. Specifically, as noted in section 6, the presence of possible adoption lags during 1971-1989 would mean that the actual innovation rate λ_1 is lower than the estimated value, which might account for the discrepancy above. In contrast to INTEL, increase in AMD’s technical efficiency also contributed to the increase in growth of performance.

To investigate the cause of increase in λ , I look at the R&D expenditures of the semiconductor equipment companies over the time period 1971-2008. The North American Industry Classification System (NAICS) classifies the semiconductor equipment manufacturing industry under a separate six digit code with the name “Semiconductor Machinery Manufacturing” (NAICS Code 333295).²⁹ The R&D expenditures of big publicly listed companies in NAICS code 333295 is available from the COMPUSTAT database.³⁰ The conclusion that emerges from the R&D expenditures of these companies is that the efficiency of R&D in the semiconductor equipment industry was higher during 1990-2008 when compared to 1971-1989. To get a measure of efficiency of R&D in the equipment industry, I assume that innovation function in the semiconductor equip-

²⁹ This industry code does not contain microprocessor manufacturers like INTEL and AMD, or manufacturers of other kinds of semiconductor chips, which are classified under NAICS Code 334413 - Semiconductor and Related Device Manufacturing

³⁰ While the data for North American companies are available for all the years of interest (1971-2008), the data for the rest of the world is available only from 1989 onwards.

Table 7: R&D EFFICIENCY IN THE SEMICONDUCTOR EQUIPMENT INDUSTRY

Companies	β		Annual R&D Growth Rate (%)	
	1971-1989	1990-2008	1971-1989	1990-2008
US Companies in NAICS Code 333295	2.29 (0.57)	0.99 (0.21)	25.9	19.6
All Companies (US + International) in NAICS Code 333295	2.29 (0.57)	1.08 (0.20)	25.9	22.1
All Companies in NAICS Code 333295 + Top Semiconductor Equipment companies not included in NAICS Code 333295	2.28 (0.57)	1.09 (0.20)	27.1	19.0

ment industry can be represented by

$$R(\ell) = R_0 \frac{1}{\ell^\beta} \quad (18)$$

where $R(\ell)$ is the R&D expenditure that the semiconductor equipment industry has to incur to invent vintage ℓ equipment. Here β is a measure of efficiency of R&D, a lower value of β implying a higher efficiency.³¹ One could think of linking this function with the Poisson assumption made in the model, but here I take a simpler approach because the results that can be derived from this approach are conclusive. I estimate the following equation for 1971-1989 and 1990-2008 separately:

$$\ln R = \beta_0 - \beta \ln \ell \quad (19)$$

The estimates are in the second and third columns in Table 7. The first row lists the estimate for β using R&D for US companies only and the second row includes R&D done by international companies also.³² As can be seen, β went down during 1990-2008 when compared to 1971-1989.

One possible criticism of this approach is that some firms in the semiconductor equipment industry that were leaders in research are not included in NAICS code 333295, either because semiconductor equipment manufacturing was only one section of their entire business or because

³¹ A lower value of β means that a smaller proportional increase in R&D is needed to produce the same proportional reduction in ℓ

³² Data is available for this subset for US companies for the entire range 1971-2008 and for international companies from 1989 onwards. Since the data for these companies are available only from 1989 onwards, I removed the observations for the year 1989 and 1990 since this would otherwise presume that the companies that were added during these years did not exist before that.

they were listed under some other category.³³ To investigate whether the above considerations are important, I compiled a list of the leading semiconductor equipment manufacturers for every year (1971-2008) using data from magazines and reports focussing on this industry. The main source is a list of top 10 revenue earners in semiconductor equipment industry released annually by VLSI research, a leading market research firm focussing on the semiconductor industry. If the revenue from semiconductor equipment manufacturing for these firms were more than 20% of total revenues then, I added the firm to the ones listed under NAICS code 333295.³⁴ The estimates of β for this bigger list of firms is shown in the third row of table. As can be seen, the result that R&D efficiency increased during 1990-2008 holds during this period as well. Since ℓ decreased by roughly the same factor, the above result should imply the R&D growth was higher during 1971-1989 when compared to 1990-2008. This is confirmed in the last two columns in Table 7, which gives the average annual R&D growth rates in the industry for the two periods.

The observation that efficiency of R&D in the semiconductor equipment industry has increased has been documented in many other sources as well (see Hutcheson (2005) and Schaller (2004)). This result suggests that to find the cause of increase in λ during 1990-2008, one must look for an explanation that hinges on an increase in R&D efficiency. Specifically this rules out competition and demand shock in the microprocessor industry as causes for increase in λ . The mechanism by which a competition or demand shock in the downstream microprocessor industry would lead to an increase in λ would presumably be one in which the semiconductor equipment firms increase their R&D expenditure growth to take advantage of the profit opportunity presented by the competition or demand shock in the microprocessor industry. The above analysis shows that the increase in λ was not accompanied by an increase in R&D growth, it was accompanied by an increase in R&D efficiency. There was in fact a decrease in R&D growth, which suggests that this could not have been the mechanism at work.

The most plausible explanation is that the increase in R&D efficiency in the semiconductor equipment industry resulted from the efforts of SEMATECH, an industrial research consortia established in 1988 with support from the US government. Concerned with the loss of dominance of US firms in the semiconductor industry during 1980s, the US government supported (through an annual subsidy) the formation of SEMATECH to accelerate innovation in US semiconductor firms. SEMATECH focused on R&D in the semiconductor equipment industry, and started issuing Technology Roadmaps stating the technological barriers to be overcome to create the next vintage of semiconductor equipment, the possible solutions, and the timeline for the semiconductor industry to move to the next vintage. The roadmap proved to be a success in the industry, and turned out to be a point of coordination for R&D among the different firms in the indus-

³³ These include companies like Perkin-Elmer, Schlumberger, Eaton, Nikon and Canon which were important innovators in semiconductor equipment manufacturing industry but are not included in NAICS code 333295 because they are big industrial conglomerates spanning many industries, and companies like Teradyne, Kulicke& Soffa and Advantest which are wholly focussed on manufacturing semiconductor equipment but are listed in other categories because of the functionality of the machines they produce.

³⁴ This led to companies like Perkin-Elmer, Nikon, Teradyne, Kulicke Soffa and Advantest being added to the list, but companies like Schlumberger and Canon were kept out. The revenue from semiconductor operations of some companies were not available for all years. For the earlier years I had to rely on data for two years, 1988 and 1989, which were available from VLSI Research (1990).

try. In a survey of technical professionals in the semiconductor industry, Schaller (2004) finds that 85% of respondents agreed that the technology roadmap "has contributed to a more regular, more predictable, and even accelerated pace of innovation through deliberate coordination of precompetitive R&D and related industry resources." Schaller (2004) concludes that "technology acceleration was cited most often as the definitive contribution of the Roadmap process". The R&D coordination activities undertaken by SEMATECH stand out as the most plausible cause of increase in λ during 1990-2008. However, further research needs to be done to find a direct cause and effect link between activities of SEMATECH and the increase in innovation rate in the semiconductor equipment industry.³⁵

While the increase in innovation rate in equipment industry explains all of the increase in growth of performance for INTEL, it only explains part of it for AMD. The increase in technical efficiency was a major cause of acceleration in AMD's performance growth. A plausible explanation for the increase in α relates to the interpretation of α as a measure of the quality of design in a microprocessor. AMD started as a second source company to INTEL, with legal right to copy and manufacture INTEL's chips.³⁶ However, INTEL refused to share the design of its chips with AMD beginning with the 80386 chip in 1986. This was followed by a long legal battle between AMD and INTEL. During this time, AMD had fallen behind INTEL in terms of improvements to the design of its microprocessors.³⁷ The early 1990s saw the settlement of the legal disputes in a series of court rulings, giving AMD the right to use 80386 and 80486 designs. With the legal problems solved, and being behind INTEL in the quality of its designs, AMD was able to release in a quick succession a series of chips that embodied new designs. This increase in design quality stands out as a possible explanation for the increase in technical efficiency α seen in AMD microprocessors during 1990s.

Although the increase in innovation rate in the semiconductor equipment industry almost fully explains the acceleration in technological progress for INTEL microprocessors in 1990s, one caveat has to be added regarding its contribution to increase in price per quality unit declines. The growth rate of microprocessor performance increased by factor of 1.79 (or 79%) for INTEL, while the decline in price per quality unit mentioned in Aizcorbe, Oliner, and Sichel (2006) increased by a factor of 2.10 (or 110%). There is a 31% difference between the changes in these two measures, and it is possible that the difference is caused by the result of decline in prices holding performance (quality) fixed.³⁸ This could have been due to INTEL reducing its prices because of competition from AMD, as suggested in Aizcorbe (2005).³⁹

³⁵ The improvements in the performance of US semiconductor equipment companies after the establishment of SEMATECH has been noted by authors, for example Macher, Mowery, and Hodges (1998) and Flamm (2007). But these authors also point out that a cause and effect relationship between these events is yet to be clearly established.

³⁶ IBM, the major customer of INTEL during most of 1970s and 1980, required INTEL to have a second supplier as a pre-condition to purchasing INTEL microprocessors.

³⁷ For example, AMD could start selling microprocessors with the 80386 design only in 1991, while INTEL had begun selling them in 1985.

³⁸ This is in line with observations in Flamm (2004) and Congressional Budget Office (2002) that increase in the rate of technological progress alone cannot explain the increase in price per quality unit declines seen in 1990s.

³⁹ It could also be that AMD's price per quality unit decline was much higher than INTEL's and since the price per quality unit declines mentioned in Aizcorbe, Oliner, and Sichel (2006) is a composite of INTEL's and AMD's, the aggregate microprocessor price index declines would be higher than that of INTEL's.

Table 8: CONTRIBUTIONS TO SLOWDOWN IN GROWTH OF MICROPROCESSOR PERFORMANCE

		INTEL	AMD
Slowdown (data)	$\frac{g_{mIII}}{g_{mII}}$	2.17	3.53
Contribution of Equipment Co.	$\frac{\lambda_{III}}{\lambda_{II}}$	1.01	1.01
Contribution of Microprocessor Co.	$\frac{1 + 2\alpha_{II}}{1 + 2\alpha_I}$	1.90	3.56

7.2 Explanation for the Slowdown

I start with the decomposition of change in growth rate in equation (17). As can be seen from Table 8, for both INTEL and AMD, there was hardly any change in the innovation rate in the equipment industry, and the decrease in g_m was caused entirely by a decline in the technical efficiency α . Given the decomposition in Table 8, the most plausible explanation of the slowdown is the one suggested in Flamm (2007). He argues that the existing stock of microprocessor design knowledge in 1990s was the outcome of research going back forty years, and had been entirely imported and absorbed into the microprocessor industry during the decade of the 1990s. Absent the knowledge to produce new innovations in design, microprocessor performance was unable to grow at the rate at which it had done previously.

In early 2000s, microprocessors with new designs introduced by INTEL hit a well publicized problem, the microprocessors generated a large amount of heat during their operation which affected their proper functioning. Since then INTEL has abandoned the pattern of design innovations that it had followed in the past. The current design trend followed by microprocessor firms INTEL and AMD is the multicore approach. This uses the additional transistors provided by new vintages of semiconductor equipment in the most direct possible way, by replicating a processor design as many times as are possible on a single chip. This approach however can speed up the execution of only those programs that are specifically written to take advantage of the parallel processing capability offered by the presence of multiple cores. Many software programmes however, are not written this way, and rewriting these applications to take advantage of the multicore design is difficult or in some cases impossible. The situation is summed up in the words of an analyst, “Running advanced multicore machines with today’s software is like putting a Ferrari engine in a go-cart” (see Barker (2009)).⁴⁰ The drop in α during 2001-2008, captures this effect, the additional transistors that INTEL and AMD are using in its new microprocessors is not making as much contribution to speeding up the execution the software programs as

⁴⁰ For a detailed technical description of the problems of developing software for multicore processors, see Asanovic, Bodik, Demmel, Keaveny, Keutzer, Kubiatowicz, Lee, Morgan, Nacula, Patterson, Sen, Wawrzyniek, Wessel, and Yelick (2008)

they previously used to.⁴¹ This explains the slowdown in growth of microprocessor performance during 2001-2008.

8 Conclusion

Four conclusions emerge from this study. First, for INTEL the acceleration in growth of performance of microprocessors during 1990-2000 was driven almost wholly by increase in innovation rate in the semiconductor equipment industry. For AMD, the acceleration in growth of performance was the combined effect of increase in innovation rate of semiconductor equipment industry and increase in the technical efficiency with which AMD used the innovations.

Second, the R&D efficiency in the semiconductor equipment industry was higher during the period of the acceleration when compared to earlier years. This suggests that the increase in innovation rate might have been the result of activities undertaken by a government supported industrial research consortia, SEMATECH, to coordinate R&D in the semiconductor equipment industry. In January 2009, major US companies focussing on battery technology approached the US government to seek subsidies to establish an R&D consortia to accelerate technology in the battery industry. Advancements in battery technology are critical to the automobile and renewable energy industries, and the companies have set SEMATECH as a model to follow. The findings in this paper suggest that SEMATECH may have played an important role in accelerating technological progress in the semiconductor industry. It points to an interesting research agenda to understand why SEMATECH was successful in the semiconductor industry and whether consortia similar to SEMATECH can have a similar impact in other industries.

Third, for both INTEL and AMD, the slowdown in technological progress during 2001-2008 was caused by a decrease in the technical efficiency of using the innovations generated by the semiconductor equipment industry. Since the inability to generate new innovations to design has affected both INTEL and AMD in a similar fashion, it is unlikely that policies for engendering more competition in the microprocessor industry can return the industry to its previous growth path of technological progress.

Fourth, innovation in the semiconductor equipment industry has been the main workhorse almost wholly driving technological progress in the microprocessor industry since 2001. However, further innovation in the semiconductor equipment industry is becoming ever more difficult as the industry approaches the physical limit to reducing the size of the transistor. If innovations in this industry slowdown, then it will accentuate the existing problems in the microprocessor industry.

⁴¹ Hardware and software companies have launched many efforts to overcome the problem of writing software that can be parallelized. In March 2007, Intel and Microsoft announced they would fund a Universal Parallel Computing Research Center (UPCRC) and invited the 25 top Computer Science departments to submit proposals. University of California, Berkeley was selected as the winner and the funding of \$10 million has resulted in the U.C. Berkeley Parallel Computing Laboratory, or Par Lab, a multidisciplinary research project for exploring the future of parallel processing.

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9 Mathematical Appendix

Proposition 1 *The optimal policy of the firm is to wait until the ratio $\frac{\bar{v}}{\bar{c}}$ falls below x^* , where*

$$x^* = \left\{ \left(\rho + \lambda - \frac{\lambda}{\delta^\varphi} \right) \left(\frac{v(1) - C(1)}{\pi_0} \right) \right\}^{\frac{1}{\varphi}}$$

Proof. The Bellman equation in 11 can be rewritten as

$$v(x) = \frac{\pi_0}{\rho + \lambda} x^\varphi + \frac{1}{\delta^\varphi} \frac{\lambda}{\rho + \lambda} [Max \{v(\delta x), v(1) - C(1)\} - v(x)]$$

where $x \in (0, 1]$. Consider operator, T that maps functions defined on $(0, 1]$ as

$$T(f(x)) = \frac{\pi_0}{\rho + \lambda} x^\varphi + \frac{1}{\delta^\varphi} \frac{\lambda}{\rho + \lambda} [Max \{f(\delta x), f(1) - C(1)\} - f(x)]$$

$T(\cdot)$ maps continuous functions to continuous functions. Moreover, it is easily seen from Blackwell's conditions that T is a contraction mapping. Hence by contraction mapping theorem there exists a unique $v(x)$ that solves the Bellman equation above. Moreover, T maps weakly increasing functions to strictly increasing functions, hence $v(x)$ is strictly increasing (see Stokey, Lucas, and Prescott (1989)). Hence, there exists a value x^* such that

$$v(x^*) = v(1) - C(1)$$

Since $v(\cdot)$ is an increasing function, $v(\delta x^*) \leq v(1) - C(1)$, since $\delta < 1$. Substituting this in Bellman equation gives

$$\begin{aligned} v(x^*) &= \frac{\pi_0}{(\rho + \lambda)} x^{*\varphi} + \frac{1}{\delta^\varphi} \frac{\lambda}{(\rho + \lambda)} Max \{v(\delta x^*), [v(1) - C(1)]\} \\ v(1) - C(1) &= \frac{\pi_0}{(\rho + \lambda)} x^{*\varphi} + \frac{1}{\delta^\varphi} \frac{\lambda}{\rho + \lambda} [v(1) - C(1)] \end{aligned}$$

which gives

$$x^* = \left\{ \left(\rho + \lambda - \frac{\lambda}{\delta^\varphi} \right) \left(\frac{v(1) - C(1)}{\pi_0} \right) \right\}^{\frac{1}{\varphi}}$$

■

Proposition 2 *There are intervals of λ over which n^* does not change.*

Proof. The adoption policy n^* depends on the threshold lag behind the technology frontier, x^* , at which the firm would adopt. Equation (12), which gives the value of x^* , however cannot be used to investigate how x^* would change with λ , because the value $v(1)$ depends on λ . Hence, I use an alternative idea to characterize how n^* depends on λ . The optimal policy n^* should give maximum expected present discounted value to the firm among all possible positive integers

$n = 1, 2, 3, \dots$. The expected present discounted value of adopting every n^{th} innovation can be calculated as follows.

Let $\{\Delta\tau_k\}_{k=0}^{\infty}$ be the adoption intervals under the optimal policy. Then the i th adoption with vintage $\ell_i = (\delta^{n^*})^i \bar{\ell}_0$, occurs at time $\tau_i = \sum_{k=0}^{i-1} \Delta\tau_k$. Then if the firm follows the policy of adopting every n th innovation, the net profit of the firm in the i th adoption interval (i.e the profit from operating the i th vintage equipment), discounted back to the beginning of the industry ($t = 0$) is:

$$\begin{aligned} \Pi_i(n, \lambda) &= e^{-\rho\tau_i} \left\{ \int_0^{\Delta\tau_i} e^{-\rho t} \frac{\pi_0}{(\delta^{ni} \bar{\ell}_0)^\varphi} dt - \frac{C(1)}{(\delta^{ni} \bar{\ell}_0)^\varphi} \right\} \\ &= e^{-\rho \sum_{k=0}^{i-1} \Delta\tau_k} \frac{1}{\delta^{ni\varphi} \bar{\ell}_0} \left\{ \frac{\pi_0}{\rho} (1 - e^{-\rho\Delta\tau_i}) - C(1) \right\} \end{aligned}$$

Let $\Pi_\infty(n)$ be the present discounted value of surplus obtained under the policy of adopting every n th innovation. Then

$$\begin{aligned} \Pi_\infty(n, \lambda) &= \sum_{i=0}^{\infty} \Pi_i(n) \\ &= \frac{1}{\bar{\ell}_0^\varphi} \left[\frac{\pi_0}{\rho} [1 - e^{-\rho\Delta\tau_0}] + \sum_{i=1}^{\infty} \frac{1}{\delta^{ni\varphi}} e^{-\rho \sum_{k=0}^{i-1} \Delta\tau_k} \left(\frac{\pi_0}{\rho} - C(1) \right) - \sum_{i=1}^{\infty} \frac{1}{\delta^{ni\varphi}} e^{-\rho \sum_{k=0}^{i-1} \Delta\tau_k} \left(\frac{\pi_0}{\rho} \right) \right] \\ &= \frac{1}{\bar{\ell}_0^\varphi} \left[\sum_{i=0}^{\infty} \frac{1}{\delta^{ni\varphi}} e^{-\rho \sum_{k=0}^{i-1} \Delta\tau_k} \frac{\pi_0}{\rho} - \sum_{i=1}^{\infty} \frac{1}{\delta^{ni\varphi}} e^{-\rho \sum_{k=0}^{i-1} \Delta\tau_k} C(1) - \sum_{i=0}^{\infty} \frac{1}{\delta^{ni\varphi}} e^{-\rho \sum_{k=0}^{i-1} \Delta\tau_k} \left(\frac{\pi_0}{\rho} \right) \right] \end{aligned}$$

Then

$$\begin{aligned} E \{ \Pi_\infty \} (n, \lambda) &= \sum_{i=0}^{\infty} E \{ \Pi_i \} (n, \lambda) \\ &= \frac{1}{\bar{\ell}_0^\varphi} \left[\sum_{i=0}^{\infty} \frac{1}{\delta^{n^*i\varphi}} \frac{\pi_0}{\rho} E \left[e^{-\rho \sum_{k=0}^{i-1} \Delta\tau_k} \right] - \sum_{i=1}^{\infty} \frac{1}{\delta^{n^*i\varphi}} C(1) E \left[e^{-\rho \sum_{k=0}^{i-1} \Delta\tau_k} \right] - \sum_{i=0}^{\infty} \frac{1}{\delta^{n^*i\varphi}} \left(\frac{\pi_0}{\rho} \right) E \left[e^{-\rho \sum_{k=0}^{i-1} \Delta\tau_k} \right] \right] \end{aligned}$$

The variables $\Delta\tau_i$ are independent draws from $\Gamma(n^*, \frac{1}{\lambda})$. It follows that

$$\sum_{k=0}^{i-1} \Delta\tau_k \sim \Gamma(n^*i, \frac{1}{\lambda})$$

To evaluate the above expectations, I use the following lemma.

Lemma 3 *If $\Delta\tau_i \sim \Gamma(n^*, \frac{1}{\lambda})$, then $E [e^{-\rho\Delta\tau_i}] = \left(\frac{\lambda}{\rho+\lambda}\right)^{n^*}$*

Proof.

$$\begin{aligned} E [e^{-\rho\Delta\tau_i}] &= \int_0^\infty e^{-\rho t} \frac{\lambda^{n^*} \Delta\tau^{n^*-1} e^{-\lambda\tau}}{\Gamma(0, n^*)} d\Delta\tau \\ &= \frac{\lambda^{n^*}}{\Gamma(0, n^*)} \frac{n^* - 1}{\rho + \lambda} \int_0^\infty \Delta\tau^{n^*-2} e^{-(\rho+\lambda)\Delta\tau} d\Delta\tau \\ &= \left(\frac{\lambda}{\rho + \lambda}\right)^{n^*} \frac{(n^* - 1)!}{\Gamma(0, n^*)} = \left(\frac{\lambda}{\rho + \lambda}\right)^{n^*} \end{aligned}$$

■

These imply that

$$\begin{aligned} E \{\Pi_\infty(n, \lambda)\} &= \sum_{i=0}^{\infty} E \{\Pi_i(n, \lambda)\} \\ &= \frac{1}{\ell_0^\varphi} \left[\sum_{i=0}^{\infty} \frac{1}{\delta^{n^*i\varphi}} \frac{\pi_0}{\rho} \left(\frac{\lambda}{\rho + \lambda}\right)^{n^*i} - \sum_{i=1}^{\infty} \frac{1}{\delta^{n^*i\varphi}} C(1) \left(\frac{\lambda}{\rho + \lambda}\right)^{n^*i} - \sum_{i=0}^{\infty} \frac{1}{\delta^{n^*i\varphi}} \left(\frac{\pi_0}{\rho}\right) \left(\frac{\lambda}{\rho + \lambda}\right)^{n^*(i+1)} \right] \end{aligned}$$

Evaluating the sums of geometric series, the above expression reduces to

$$E \{\Pi_\infty(n, \lambda)\} = \frac{1}{\ell_0^\varphi} \left[\frac{\left\{1 - \left(\frac{\lambda}{\rho + \lambda}\right)^n\right\} \frac{\pi_0}{\rho} - \left(\frac{1}{\delta^\varphi} \frac{\lambda}{\rho + \lambda}\right)^n C(1)}{1 - \left(\frac{1}{\delta^\varphi} \frac{\lambda}{\rho + \lambda}\right)^n} \right]$$

Hence n^* should satisfy

$$n^* = \underset{n}{\operatorname{argmax}} E \{\Pi_\infty(n, \lambda)\}$$

and the value of n that solves the problem above is the optimal value n^* . It is easy to verify that the maximand evaluated at n^* is the optimal value of the firm $\frac{1}{\ell_0^\varphi} v(1)$. Since optimal policy is

to adopt every n^* th innovation, the following equations should hold, Since the firm adopts a new linewidth at every n^* th innovation, the following equations must hold

$$\begin{aligned}
(\rho + \lambda)v(1) &= \pi_0 + \frac{\lambda}{\delta^\varphi}v(\delta) \\
(\rho + \lambda)v(\delta) &= \delta^\varphi\pi_0 + \frac{\lambda}{\delta^\varphi}v(\delta^2) \\
&\vdots \\
(\rho + \lambda)v(\delta^{n^*-2}) &= \delta^{(n^*-2)\varphi}\pi_0 + \frac{\lambda}{\delta^\varphi}v(\delta^{n^*-1}) \\
(\rho + \lambda)v(\delta^{n^*-1}) &= \delta^{(n^*-1)\varphi}\pi_0 + \frac{\lambda}{\delta^\varphi}[v(1) - C(1)]
\end{aligned}$$

Repeatedly substituting from the last to the first gives,

$$\begin{aligned}
\frac{1}{\ell_0^\varphi}v(1) &= \frac{1}{\ell_0^\varphi} \left[\frac{\left\{ 1 - \left(\frac{\lambda}{\rho + \lambda} \right)^{n^*} \right\} \frac{\pi_0}{\rho} - \left(\frac{1}{\delta^\varphi} \frac{\lambda}{\rho + \lambda} \right)^{n^*} C(1)}{1 - \left(\frac{1}{\delta^\varphi} \frac{\lambda}{\rho + \lambda} \right)^{n^*}} \right] \\
&= E \{ \Pi_\infty(n^*, \lambda) \}
\end{aligned}$$

Hence to investigate how n^* changes with λ it is enough to see how the n that solves the above problem changes with λ . It can be seen from the above expression that $E \{ \Pi_\infty(n, \lambda) \}$ is increasing in λ as long as

$$\frac{1}{(\delta^\varphi)^n} \left[\frac{\pi_0}{\rho} - C(1) \right] > \frac{\pi_0}{\rho}$$

The above condition is intuitive. The net profit from adopting, the left hand side, should be greater than the present discounted value of the infinite stream of profits the firm gets if it never adopts, which is the right hand side. The diagram below illustrates how the optimal n changes with λ . Each curve is the maximand in the above problem for a given n . As can be seen from the graph, there is a range of values λ for which a given n is optimal. When λ increases beyond this range, the optimal n jumps up by one.

■

Proposition 4 Consider two samples of size N_1 and N_2 drawn from gamma distributions $\mathbf{G}(n^*, \frac{1}{\lambda_1})$ and $\mathbf{G}(n^*, \frac{1}{\lambda_2})$ respectively. Then

$$\frac{\Delta \bar{\tau}_1}{\Delta \bar{\tau}_2} \sim \mathbf{F}(2n^*N_1, 2n^*N_2) \tag{20}$$

if $(\lambda_1 = \lambda_2)$

Proof. Consider two samples of size N_1 and N_2 drawn from gamma distributions $\mathbf{G}(n^*, \frac{1}{\lambda_1})$ and $\mathbf{G}(n^*, \frac{1}{\lambda_2})$ respectively. Let $\tau_{ij}, j = 1, 2, 3..N_i$, be random variables representing draws from the

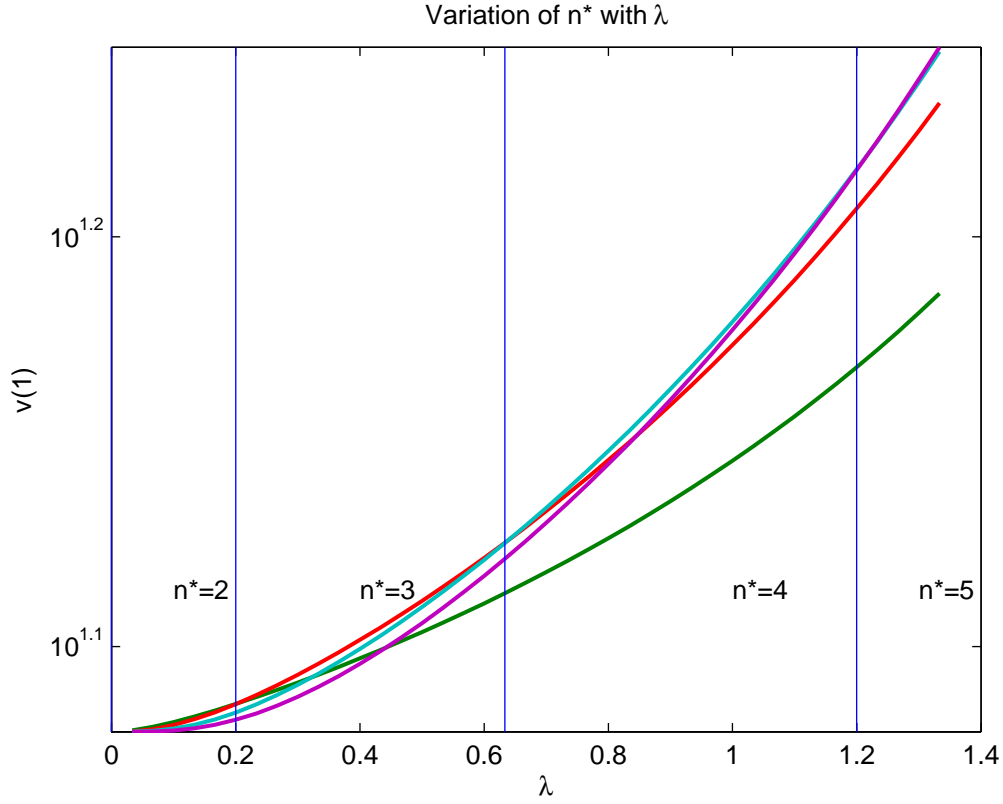


Figure 4: Variation of n^* with λ

two distributions $i \in \{1, 2\}$. Then from the scaling property of the gamma distribution, $2\lambda_i\tau_i \sim \mathbf{G}(n^*, 2)$. From the property of sum of gamma distributed variables, $2 \sum_{j=1}^{N_i} \lambda_i\tau_{ij} \sim \mathbf{G}(n^*N_i, 2)$. But $\mathbf{G}(n^*N_i, 2)$ is the same as $\chi^2(2n^*N_i)$, the chi-square distribution with $2n^*N_i$ degrees of freedom. Hence $2 \sum_{j=1}^{N_i} \lambda_i\tau_i \sim \chi^2(2n^*N_i)$. Since the ratio of χ^2 variables (normalized by the degrees of freedom) follows an \mathbf{F} distribution,

$$\frac{2 \sum_{j=1}^{N_1} \lambda_1\tau_{1j}/N_1}{2 \sum_{j=2}^{N_2} \lambda_2\tau_{2j}/N_2} \sim \mathbf{F}(2n^*N_1, 2n^*N_2)$$

Under the null hypothesis of $\lambda_1 = \lambda_2$, the above equation reduces to

$$\frac{\sum_{j=1}^{N_1} \tau_{1j}/N_1}{\sum_{j=1}^{N_2} \tau_{2j}/N_2} \sim \mathbf{F}(2n^*N_1, 2n^*N_2)$$

or equivalently,

$$\frac{\bar{\tau}_1}{\bar{\tau}_2} \sim \mathbf{F}(2n^*N_1, 2n^*N_2) \quad (21)$$

■

Proposition 5 If $\{\Delta\tau_i\}_{i=0}^N$ are N independent draws from the gamma distribution, $\Delta\tau_i \sim \mathbf{G}(n^*, \frac{1}{\lambda})$, then the maximum likelihood estimates $\hat{\lambda}$ and \hat{n}^* should satisfy $\hat{\lambda} = \frac{\hat{n}^*}{\Delta\bar{\tau}}$, where $\Delta\bar{\tau}$ is the mean

of the observations, $\Delta\bar{\tau} = \frac{\sum_{i=1}^N \tau_i}{N}$.

Proof. Let $\{\Delta\tau_i\}_{i=0}^N$ represent N observations on adoption intervals with $\Delta\tau_i \sim \mathbf{G}(n^*, \frac{1}{\lambda})$. Using the p.d.f for gamma distribution, the probability that these N observations are drawn from $\mathbf{G}(n^*, \frac{1}{\lambda})$ is

$$\prod_{i=1}^N g(\Delta\tau_j) = \prod_{i=1}^N \frac{\lambda^{n^*} \Delta\tau_i^{n^*-1} e^{-\lambda\Delta\tau_i}}{\Gamma(0, n^*)}$$

The log-likelihood function is then

$$\begin{aligned} L(n^*, \lambda) &= \sum_{i=1}^N \{-\ln[\Gamma(0, n^*)] + n^* \ln(\lambda) + (n^* - 1) \ln(\Delta\tau_i) - \lambda\tau_i\} \\ &= -N \ln[\Gamma(0, n^*)] + Nn^* \ln(\lambda) + (n^* - 1) \sum_{i=1}^N \ln(\Delta\tau_i) - \lambda \sum_{i=1}^N \Delta\tau_i \end{aligned}$$

Let $\hat{n}^*, \hat{\lambda}$ be the MLE estimates. Then

$$\frac{\partial L}{\partial \lambda}(\hat{n}^*, \hat{\lambda}) = 0$$

which gives $\frac{N\hat{n}^*}{\hat{\lambda}} - \sum_{i=1}^N \Delta\tau_i = 0$ and hence $\hat{\lambda} = \frac{N\hat{n}^*}{\sum_{i=1}^N \Delta\tau_i}$. Hence the MLE estimates can be calculated by a simple procedure. For every positive integer n , find the optimal λ using the condition above. Then choose the $(\hat{n}^*, \hat{\lambda})$ pair that maximizes the likelihood function above. ■

10 Data Appendix

10.1 Description of the Dataset

The dataset constructed in this paper spans the time period 1971-2008. The data contains time series of characteristics of all INTEL and AMD desktop and laptop microprocessors, starting with the first microprocessor in 1971. There is a total of 588 microprocessors for INTEL and 457 for AMD. These contain desktop and laptop microprocessors produced by INTEL. Among these, 135 microprocessors are in the low value category, which INTEL sells under the name Celeron microprocessors. These are usually defective parts which are sold at a low price. Hence I omit these microprocessors in this paper. This leaves a total of 453 microprocessors for INTEL and 351 for AMD.

The dataset contains the following characteristics for each microprocessor - product name, date of release, performance (m), vintage (ℓ), transistors (T), and size (S). The date of adoption of a vintage by a firm is taken to be the date of release of the first microprocessor using that vintage, by the firm. The data for all variables except m , is available for each microprocessor. Table 9 gives the number of microprocessors in each market segment, and the number of microprocessors in each category for which data for m is available. Table 11 lists all the data sources and provides an abbreviation for each source. Table 12 lists the specific data sources for each variable.

Table 9: MICROPROCESSORS IN THE DATASET

Category	INTEL		AMD	
	Total	m Available	Total	m Available
Desktop microprocessors	204	173	251	168
Laptop microprocessors	249	120	97	20
Total	453	293		

Table 10 breaks up the microprocessors in the dataset by vintage.

Table 10: MICROPROCESSORS IN THE DATASET BY VINTAGE

Vintage	INTEL		AMD	
	Total	m Available	Total	m Available
10.000 μ	2	2	0	0
6.000 μ	1	1	1	1
3.000 μ	5	5	6	4
1.500 μ	6	6	3	3
1.000 μ	5	4		
0.800 μ	9	9	5	4
0.700 μ			5	5
0.600 μ	9	9		
0.500 μ			5	5
0.350 μ	22	20	5	5
0.250 μ	24	15	20	17
0.180 μ	37	33	49	30
0.130 μ	83	54	81	37
0.090 μ	67	49	89	39
0.065 μ	125	58	69	29
0.045 μ	58	23	7	6
Total	440	293	345	

10.2 Construction of the Performance Data Series

Since performance m is the most important time series used in this paper, I describe its construction in detail. The main source for performance data is SPEC. The SPEC numbers are not available for all microprocessors, hence I use two additional sources - MIPS rating and SYS-MARK rating from BAPCO. In addition, the SPEC standard itself has undergone 4 revisions, SPEC-1992, SPEC-1995, SPEC-2000 and SPEC-2006. SPEC also gives 2 performance numbers, SPECINT and SPECFP. The former is a performance measure for Integer Operations and the latter for Floating Point Operations. These different ratings were converted into a single standard, SPEC-00, according to the procedure below.

First, the SPECINT and SPECFP ratings for each microprocessor was combined in the ratio 4:1 to arrive at a single SPEC rating. The ratio 4:1 has been suggested as good weights for the mixture of integer and floating point operations used on average. The SPECINT and SPECFP numbers are however highly correlated and hence the weights do not have much effect on the growth rate of the weighted series.

Table 11: ABBREVIATION FOR DATA SOURCES

Source	Abbreviation
1 INTEL microprocessor Quick Reference Guide, at (http://)	INT-QR
2 Standard Performance Evaluation Corporation, at (http://)	SPEC
3 BAPCO , at (http://)	BAPCO
4 Market Research Reports from INSTAT CAHNERS	INSTAT
5 Dataset from Semiconductor Marketing Associates	SMA
6 Dataset from IC Knowledge	IC-KNOWLEDGE
7 CPU World , at (http://)	CPU-WORLD
8 Sandpile , at (http://www.sandpile.org)	SANDPILE
9 Dataset from Prof.Mark Horowitz and Francois Labonte, at (http://)	HOROWITZ-LABONTE

Table 12: DATA SOURCES FOR EACH VARIABLE

Variable	Symbol	Source
List of Microprocessors	-	INT-QR, CPU-WORLD, SANDPILE.
Date of Release :	-	INT-QR, CPU-WORLD, SANDPILE.
Performance	m	SPEC, BAPCO, HOROWITZ-LABONTE, ANAND-TECH
Vintage:	ℓ	INTEL-QR, HOROWITZ-LABONTE, INSTAT, IC-KNOWLEDGE.
Transistors:	T	INTEL-QR, HOROWITZ-LABONTE, INSTAT, SANDPILE
Size:	S	HOROWITZ-LABONTE, INSTAT, SANDPILE, CPU-WORLD.
Defect Density	σ	IC-KNOWLEDGE

Second, for each pair of ratings that were used in close periods of time, like SPEC-92 and SPEC-96 or MIPS and SPEC-92, there is a usually a set of microprocessors for which data for both the ratings are available. I used the data from this common set of microprocessors to find conversion factors between the two ratings. The conversion factor I used was the average of the ratio between the performance numbers in both standards for the same microprocessor. The ratios are usually the same across microprocessors, indicating that this procedure is fairly accurate. The conversion factor between the series are listed in Table 13.

The conversion numbers between the SPEC ratings in this paper are close to the ones reported in Nordhaus (2001), who converts different measures into a standards he defines as MSOPS

Table 13: CONVERSION FACTORS

Standard 1	Standard 2	Conversion Factor
MIPS	SPECINT-92	0.78
SPECINT-92	SPECINT-95	0.02
SPECINT-95	SPECINT-00	9.80
SPECINT-00	SPECINT-06	160.15
SPECFP-92	SPECFP-95	0.02
SPECFP-95	SPECFP-00	10.00
SPECFP-00	SPECFP-06	174.47
BAPCO SYSMARK -02	SPEC-00	3.49
BAPCO SYSMARK -04	SPEC-00	6.91
BAPCO SYSMARK -07	SPEC-00	19.35
BAPCO MOBILEMARK - 02	SPEC-00	7.01
BAPCO MOBILEMARK - 07	SPEC-00	11.85

(Millions of Standardized Operations per Second).

Table 14: DATA FOR TEST OF HYPOTHESIS (i)

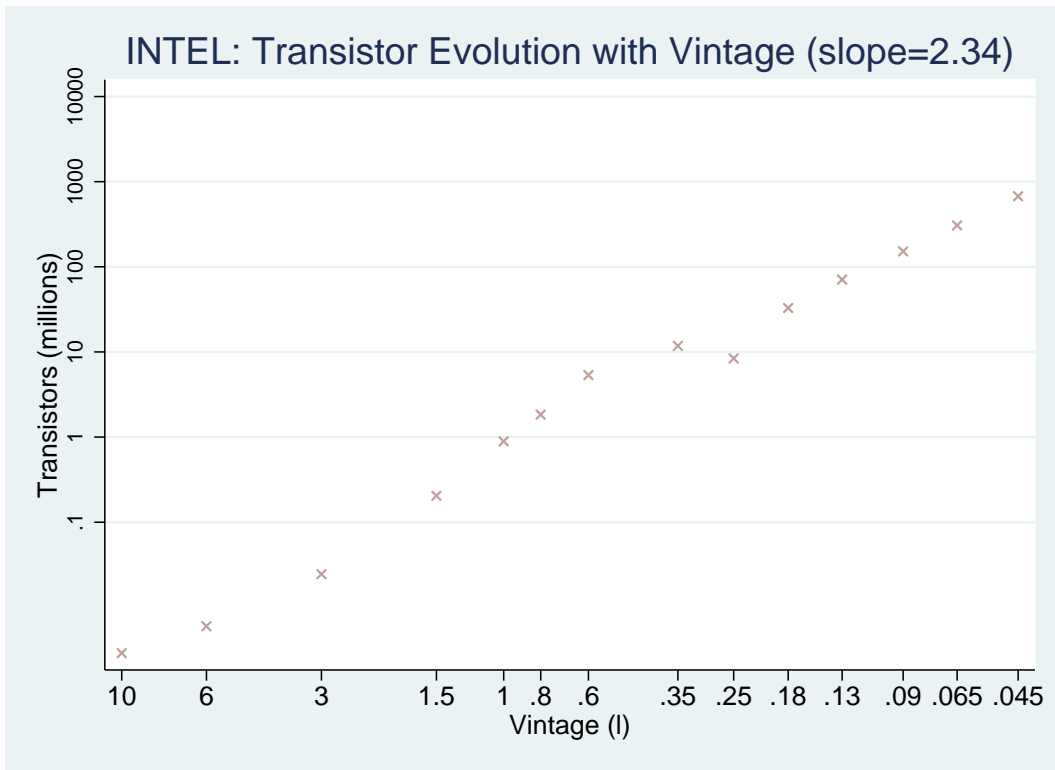
Period	Vintage ℓ	Microprocessor	Date of Adoption	Adoption Interval τ_k (in years)
1971-1989	10μ	4004	15 November 1971	-
	6μ	8080	1 April 1974	2.378
	3μ	8085	1 March 1976	1.918
	1.5μ	286 - 10	1 Feb 1982	5.926
	1μ	386-DX 33	10 April 1989	7.192
1990-2000	0.8μ	486-DX 50	24 June 1991	2.206
	0.6μ	486-DX4 100	7 March 1994	2.704
	0.35μ	Pentium 120	27 March 1995	1.055
	0.25μ	Pentium II 333	26 Jan 1998	2.838
	0.18μ	Pentium III 650	25 Oct 1999	1.745
2001-2008	0.13μ	Pentium III 1133	30 June 2001	1.682
	0.09μ	Pentium 4 HT 3.2E	1 Feb 2004	2.592
	0.065μ	Pentium D 940	16 Jan 2006	1.959
	0.045μ	Core 2 Duo E8500	20 Jan 2008	2.011

Table 15: DATA FOR TEST OF HYPOTHESIS (ii)

Period	Vintage (ℓ)	Performance (m)	
		INTEL	AMD
1971-1989	10μ	0.009	
	6μ	0.09	0.09
	3μ	0.08	0.09
	1.5μ	0.58	0.27
	1μ	2.45	
1990-2000	0.8μ	7.96	1.4
	0.7μ		3.19
	0.6μ	25.03	
	0.5μ		10.62
	0.35μ	63.70	32.91
	0.30μ		52.17
	0.25μ	162.48	151.15
	0.18μ	411.71	418.03
2001-2008	0.13μ	1057.34	1081.56
	0.09μ	1530.35	1603.27
	0.065μ	2290.01	1974.06
	0.045μ	3395.16	3428.33

Figure 5: Transistors increase at twice the rate at which ℓ decreases.

(a) INTEL



(b) AMD

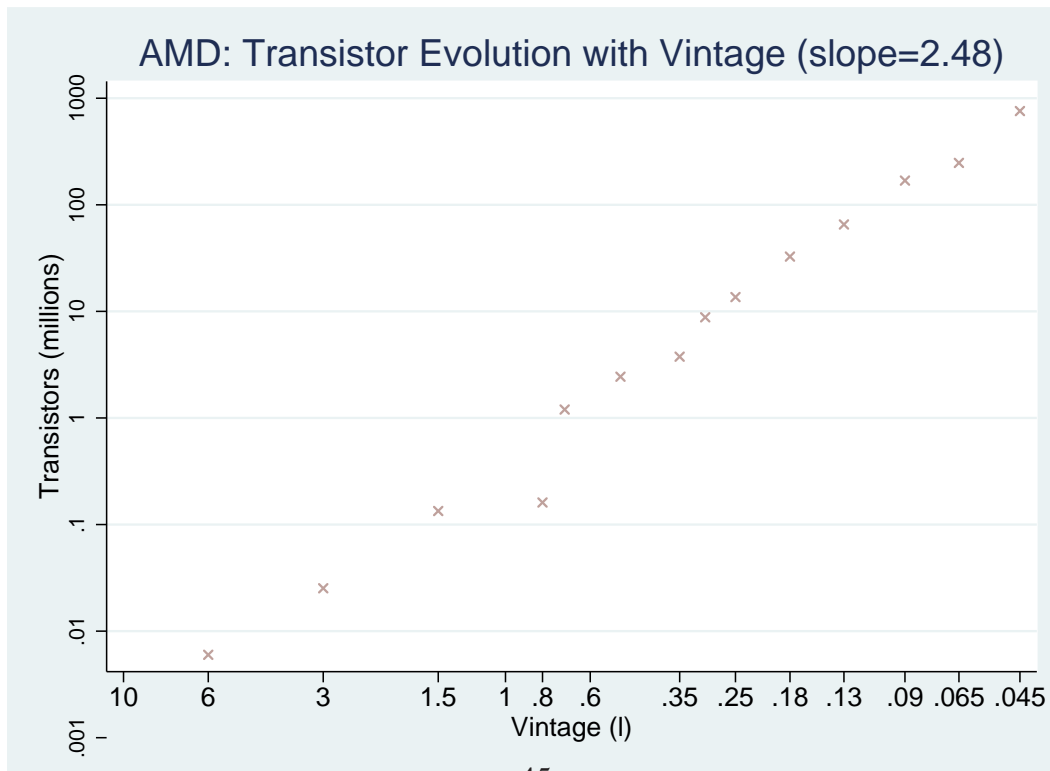
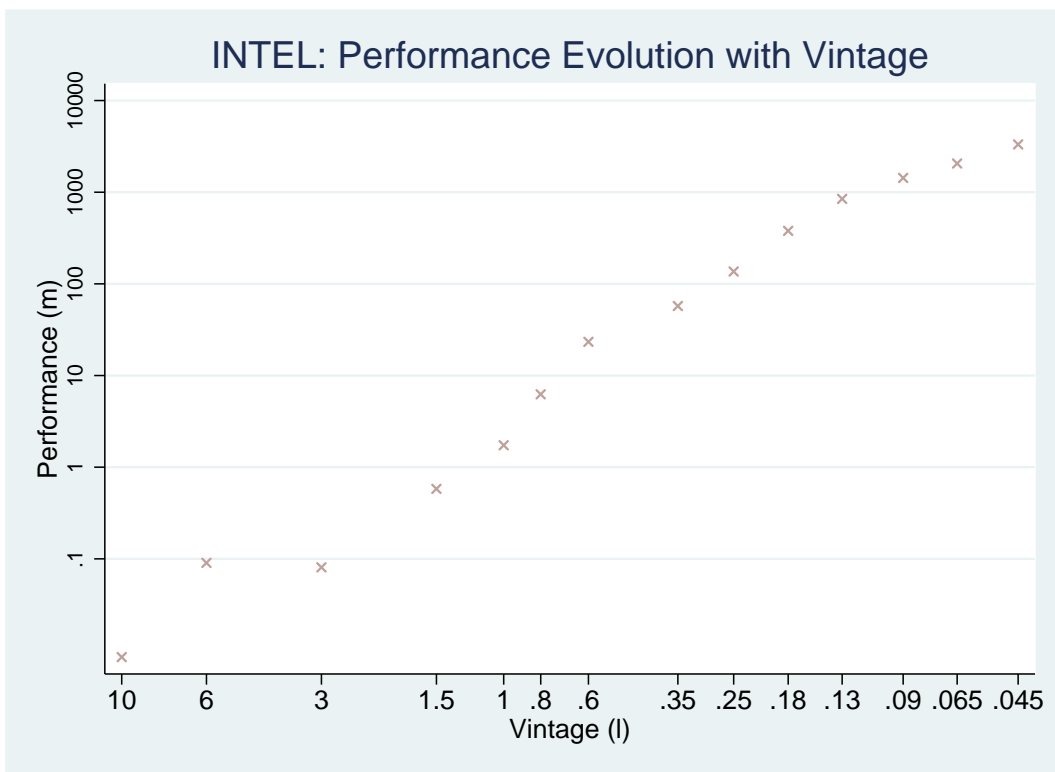


Figure 6: Performance increases as ℓ decreases.

(a) INTEL



(b) AMD

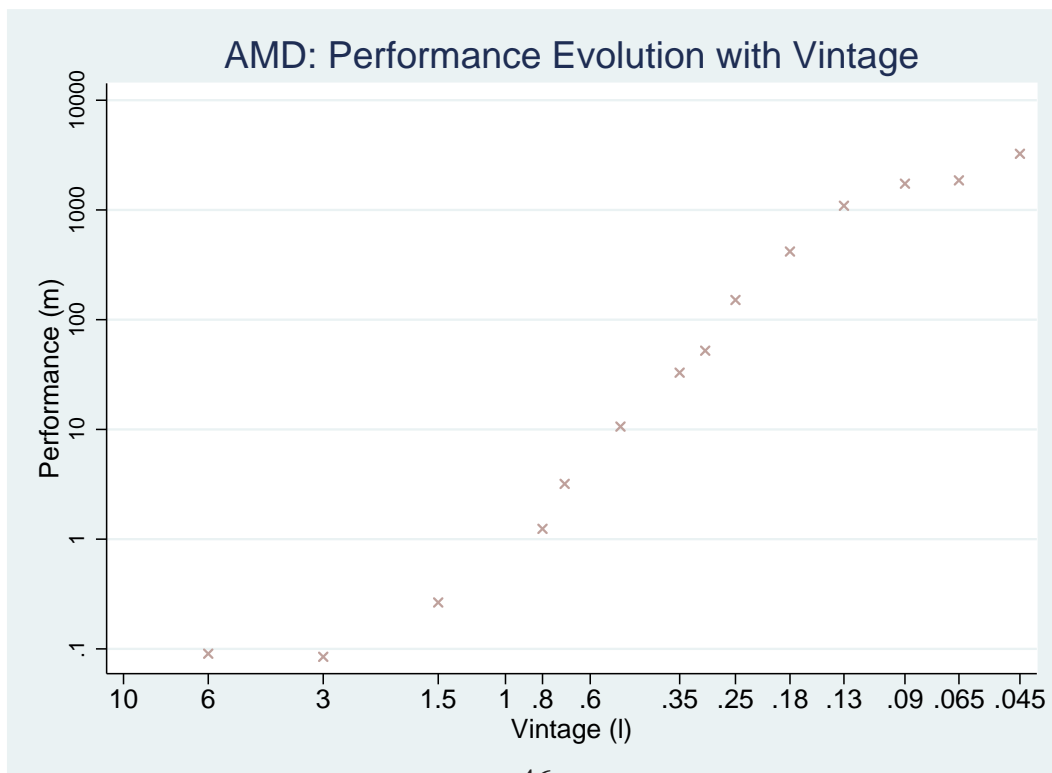
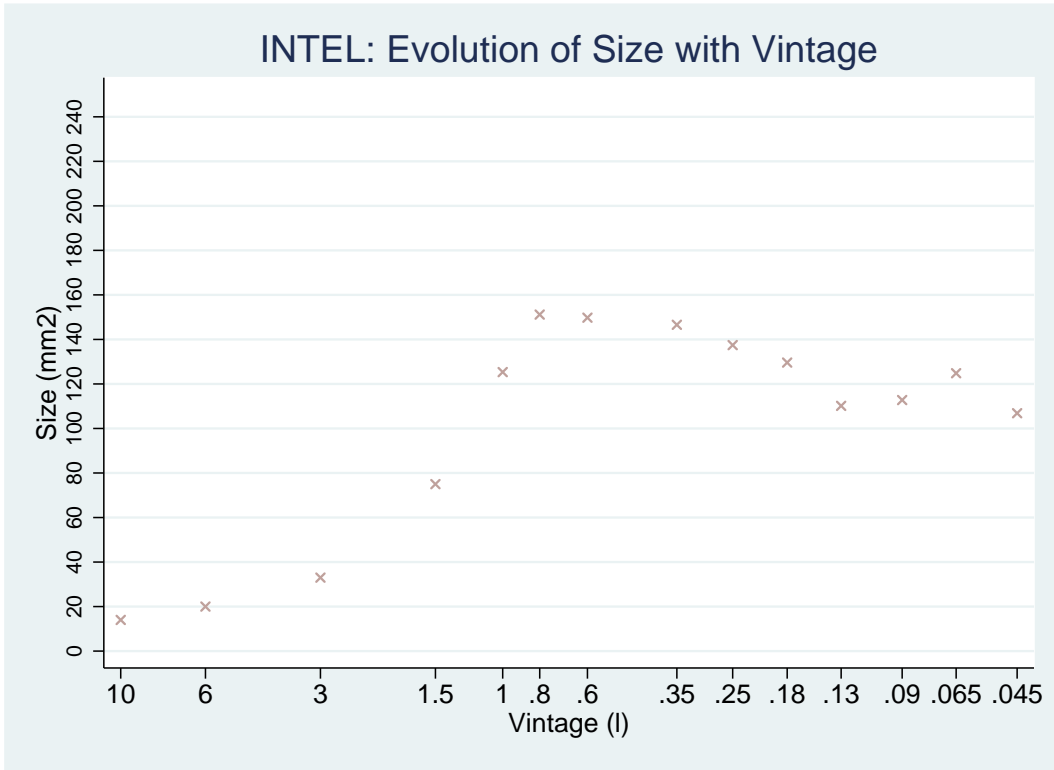


Figure 7: Size does not show any systematic trend with ℓ .

(a) INTEL



(b) AMD

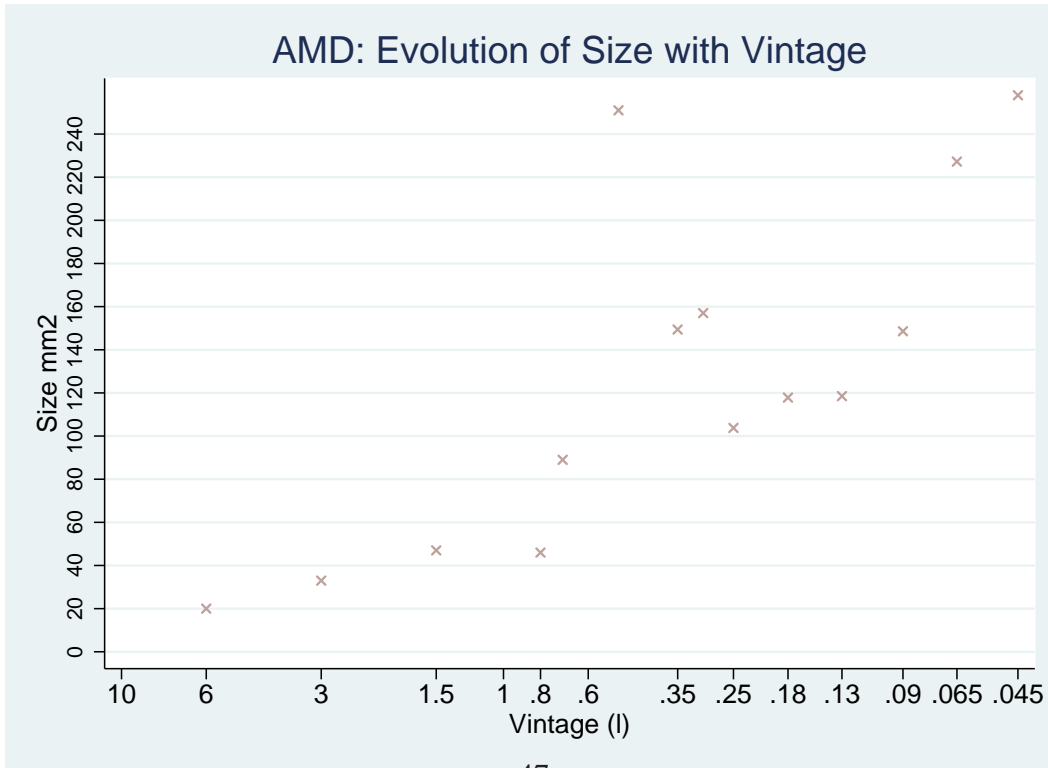
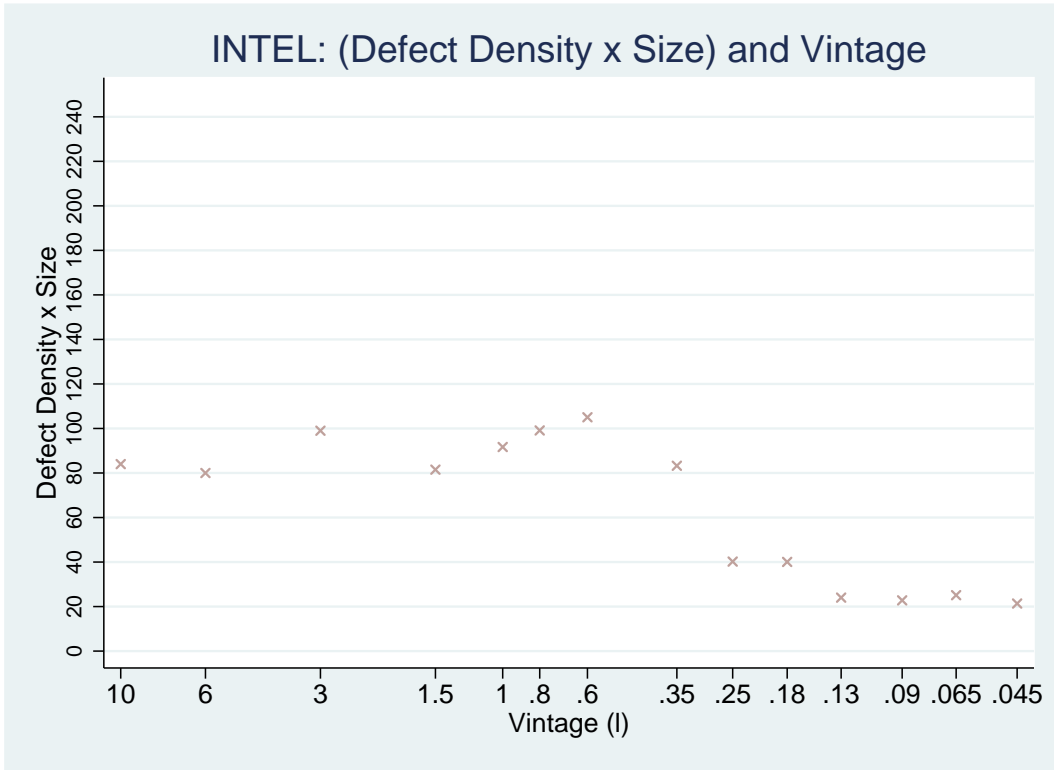


Figure 8: Size does not show any systematic trend with ℓ .

(a) INTEL



(b) AMD

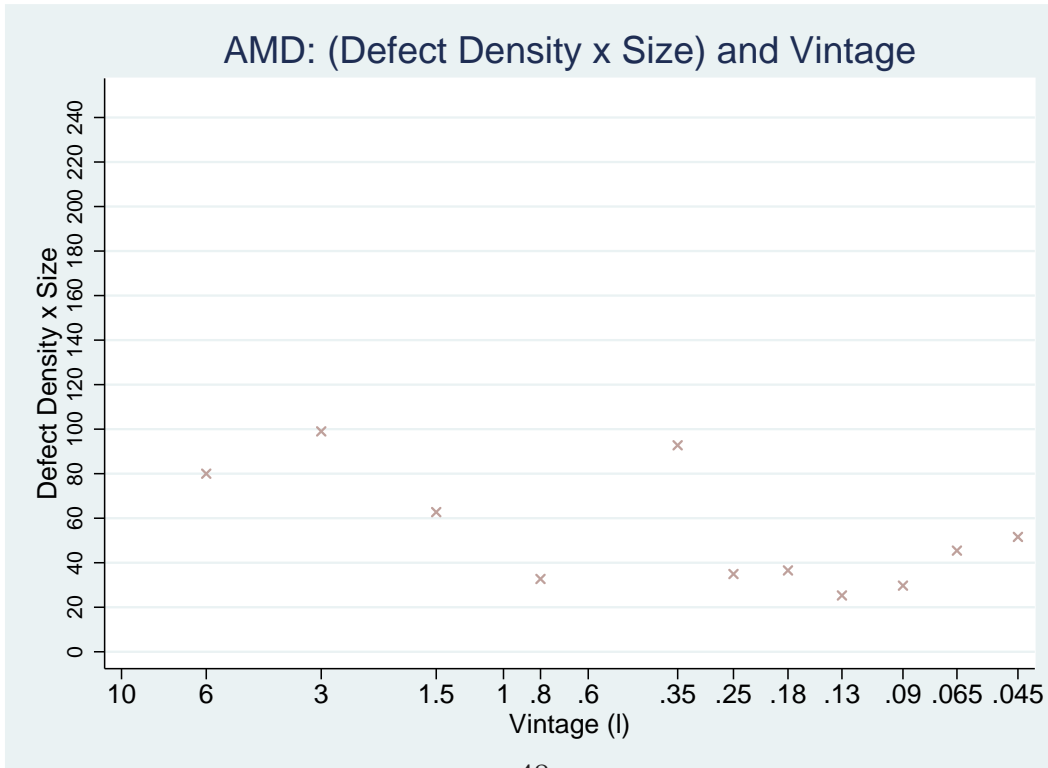
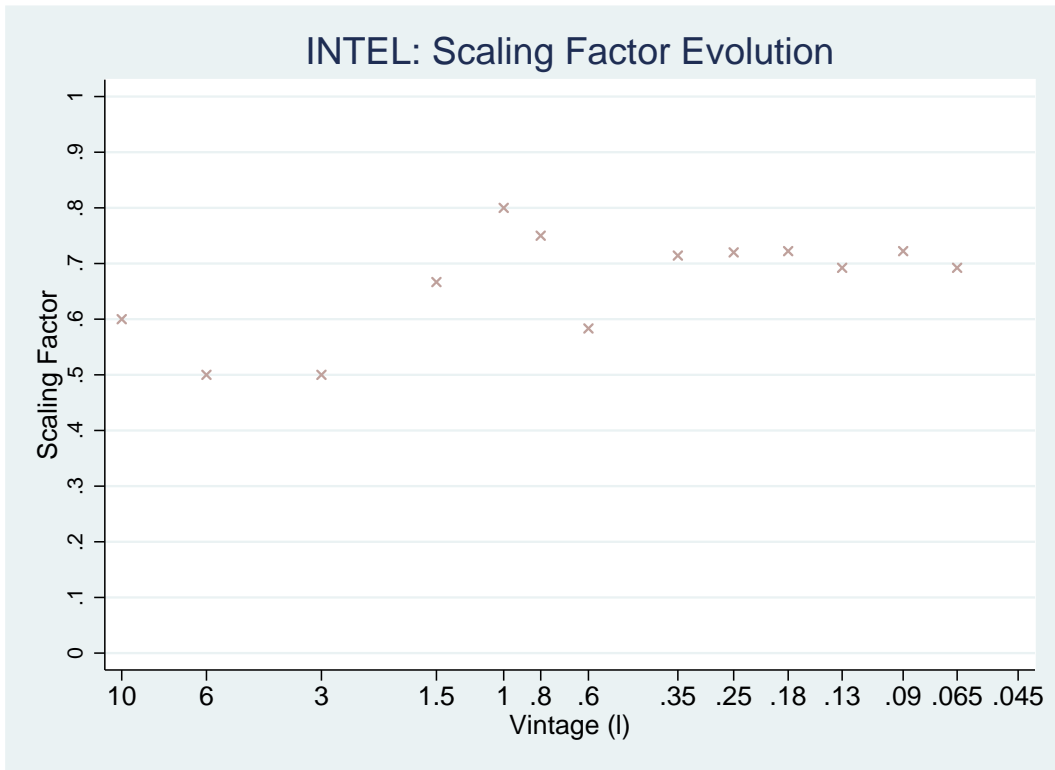


Figure 9: Factor by which ℓ scales does not show any systematic variation with ℓ .

(a) INTEL



(b) AMD

